Hybrid Si/SiC Switch Modulation with Minimum SiC MOSFET Conduction in Grid Connected Voltage Source Converters

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Abstract—In this paper a hybrid Si/SiC switch (HyS) modulation with minimum SiC MOSFET conduction (mcHyS) is experimentally characterized so to derive its conduction and switching performance. These are later used to derive a silicon area analytical model for the HyS configuration. The chip area model is used to benchmark the mcHyS modulation concepts against single technology switches and typical HyS modulation, when considering the implementation of a 100 kW two-level Voltage Source Converter (VSC) deployed for three industrial applications: photovoltaic inverter, electric vehicle fast-charging station, and battery storage systems for grid ancillary service.

The two additional switching events of the SiC MOSFET, which differentiate the mcHyS modulation from the typical HyS one, are proven to happen in soft switching, therefore the mcHyS switching performances are not penalized. Furthermore, the analysis presented shows how the studied mcHyS modulation performs against the single semiconductor technology and the typical HyS solution, in terms of cost and power conversion efficiency. More specifically, it is shown that the HyS solutions are particularly competitive versus the full Si-based VSCs when the application at hand often operates at low partial loads. Finally, a 10kW two-level VSC assembled with mcHyS is tested so to compare its efficiency versus single technology switches.

Index Terms—Hybrid Si/SiC switch, Double Pulse Test, SiC MOSFET, Grid connected Voltage Source Converter.

I. Introduction

SILICON (Si) IGBTs are currently the dominant power semiconductor technology for industrialized high power grid-connected Voltage Source Converters (VSCs), due to their robustness, relatively low cost, and good conduction performance at high currents [1]. Nonetheless, Si IGBTs have unsatisfactory performance at low current conditions, e.g., partial load efficiency, and, especially in high voltage class devices, the current tail observed during IGBTs turn-off results in high switching losses [2]. In this context, silicon carbide (SiC) MOSFETs have gained popularity due to their excellent switching performance, the easy paralleling feature that can enable a higher power handling, and, above all, the higher temperature capability of the SiC material, which can simplify the thermal management of the system [3]–[5]. The major drawback of the SiC MOSFET is the higher manufacturing cost and unproven reliability when compared to the traditional Si IGBT [6]. The significantly higher cost of the SiC MOSFET calls for a compromised solution, e.g., a hybrid Si/SiC switch (HyS).

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HySs are typically implemented by paralleling Si IGBTs and SiC MOSFETs, employing the excellent conduction and switching characteristics of the unipolar SiC devices to reduce the overall losses with respect to IGBTs [2], [7]–[9]. Various aspects of this HyS concept, such as current sharing and performance modelling [10], [11], switching strategy [12]–[14], fault tolerance [15], [16], and the influence of the parasitic inductance in the switching performances [12], have been investigated. Overall, HySs have demonstrated promising performances in several power electronics applications, including in aircraft's high speed drives [17], wireless power transfer systems [18], and grid connected inverters [19], while offering a compromised cost solution between full Si and SiC-based switches.

An alternative HyS concept with minimum SiC MOSFET conduction (mcHyS) foresees the SiC MOSFETs acting only during the switching transitions and then being kept off during the main current conduction period. This HyS concept, shown together with its corresponding switching pattern in Fig. 1, may allow a further cost reduction since it allows the SiC device to have minimum conduction losses and therefore require a small chip area. In this HyS arrangement, the addition of an anti-parallel diode is necessary, so to conduct the reverse current which otherwise would only be conducted by the body-diode and the small chip area, i.e. MOSFET channel in reverse direction, leading to unsatisfactory loss performance due to the high voltage drop. A comparison between the HyS with minimum SiC MOSFET conduction and the typical HyS implementation (tHyS), which foresees SiC MOSFET to share the conducted current with the Si IGBT, has been described in [20], [21]. However, these studies did not consider in depth its modeling, performance analysis, and the chip area
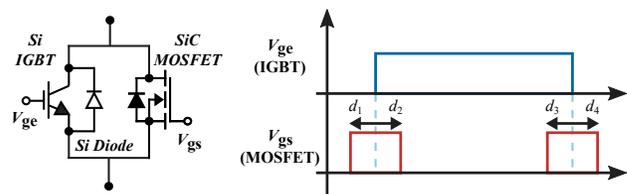

Fig. 1. Circuit schematic and switching pattern of the HyS with minimum SiC MOSFET conduction, consisting of paralleling Si IGBT with SiC MOSFET, with the SiC MOSFET aiming solely the enhancement of switching performance. Note that the switching strategy can be optimized by the proper selection of the switching delays $d_1...d_4$.
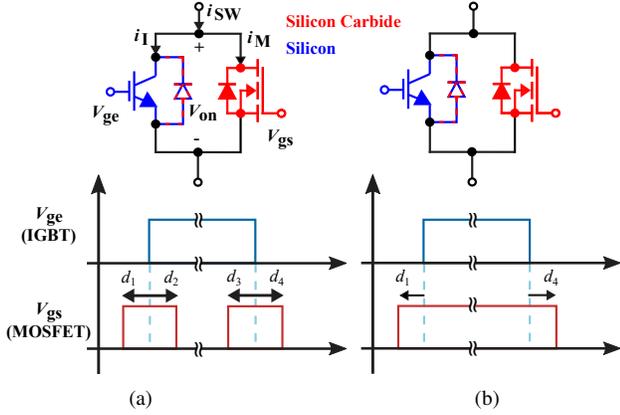
Fig. 2. Si/SiC HyS arrangements and switching patterns: (a) mcHyS where the SiC MOSFET used for the switching transition only, and (b) tHyS where the SiC MOSFET used both for the switching transitions and for sharing the current conducted by the switch with the Si IGBT.

optimization, which are fundamental to properly gain insights on their performance and cost behavior when compared to commercial Si and SiC-based switches, and so to assess their suitability in industrial applications.

In this paper the mcHyS, as well as the other switch arrangements, tHyS, SiC MOSFET and Si IGBT are experimentally characterized through Double Pulse Testing (DPT) hardware platform so to derive their conduction and switching performance. Furthermore, a 10kW two-level Voltage Source Converter (2L-VSC) assembled with mcHyS is tested so to compare its efficiency versus single technology switches. Based on the DPT characterization a silicon area analytical model for the conceptualization of HyS switch configurations, is derived. Then, the developed models are used to benchmark the mcHyS concept, against the tHyS implementation and the traditional full Si and SiC-based switches. Herein, the device chip area is optimized deriving highly utilized solutions for cost competitiveness of the studied mcHyS operations. Furthermore, the mcHyS, with a 1200 V voltage class, is compared when implemented in a 100 kW 2L-VSC deployed in various applications, such as photovoltaic (PV) inverter, electric vehicle (EV) fast-charging station (FCS), and battery energy storage systems (BESS) providing grid ancillary service, therefore aiming at investigating its suitability on actual power electronics applications. These applications are selected due to their relevance in the modern electricity system, and also because they require different operation of the 2L-VSC: in solar application the VSC acts primarily as inverter, in EV FCSs the converter acts as rectifier, and in energy storage application the bidirectional operation is needed.

The contributions of the paper are:

- The analytical modelling, experimental characterization, and the digital control implementation in a 10kW 2L-VSC of the mcHyS modulation shown in Fig. 1.
- The generalized silicon area analytical model for the conceptualization of HySs featuring minimum cost and high utilization of each switch technology for a cost-performance comparison of the HyS concepts.
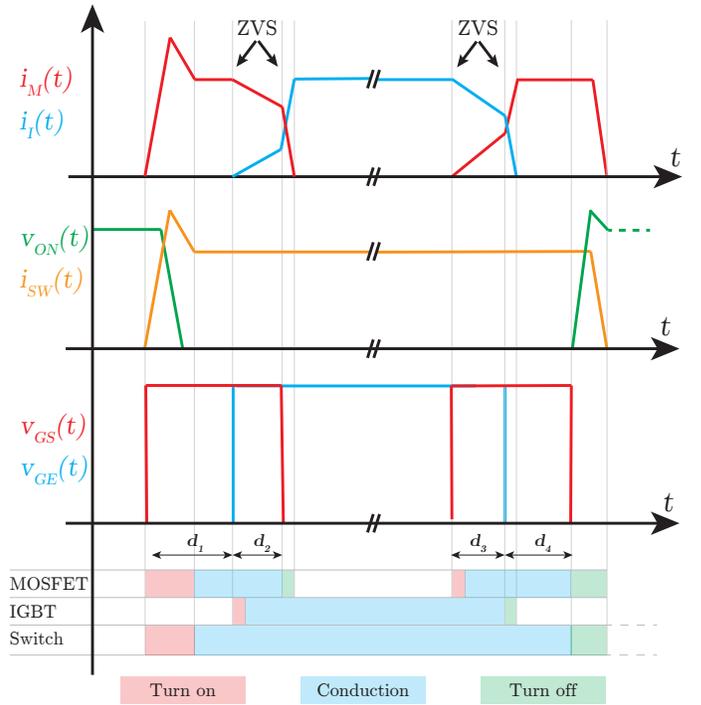

Fig. 3. Commutation process of the mcHyS. The switching transitions and conduction periods are highlighted with different colors and the currents and voltages are referred to the schematic of Fig. 2(a).

- The benchmarking of the mcHyS versus the other switch technologies in the grid-connected application of PV inverter, EV FCS, and BESS converter.

The remainder of the paper is organized as follows. Section II describes the HyS arrangements and details the commutation process of the mcHyS. Section III provides the analytical models of 2L-VSCs based on the five switch configurations (mcHyS, tHyS, Si IGBT, and SiC MOSFET), and Section IV details the HyS experimental characterization. The switch chip area and cost optimization procedure is described in Section V, and based on this, in Section VI, the different switches are compared when adopted in grid-connected applications and the limitations of mcHyS are discusses. The concluding remarks are given in Section VII.

II. HYBRID SI/SIC SWITCHES

The assembly of Si/SiC HySs is realized paralleling a Silicon based device with a Silicon Carbide based one. The possible structures and modulation pattern are shown in Fig. 2. The tHyS assembly and modulation is shown in Fig. 2 (b). Here, a SiC MOSFET is paralleled to a Si IGBT, both to facilitate the switching transition and to share the conducting current. Such configuration, previously studied in literature [10]–[12], has shown to be well performing from both the conduction and switching losses point of view, placing itself in between the pure Si IGBT and SiC MOSFET in the cost efficiency matrix. In the tHyS the addition of a parallel diode is not strictly necessary. However, especially in grid connected application that require high reactive power operation and particularly during startup when all switches are kept off,

it is useful to share the reverse conducting current with an anti-parallel diode, otherwise the SiC-MOSFET would have to be rated to withstand a high current, therefore losing its cost competitiveness.

The HyS with minimum SiC MOSFET conduction, mcHyS, shown in Fig. 2 (a), is an alternative configuration for an HyS. The key difference from the tHyS consists in the switching pattern. The detailed commutation process of the mcHyS is shown in Fig. 3, where it can be seen that switching losses occur only in the first and last MOSFET commutation, since the other switching events occur with the switch already on and so with ZVS soft switching because the parallel association is already conducting the impressed AC current and the voltage across the switch is very small. The delays $d_1...d_4$ can be optimized so to enhance the switching and conduction performances of the mcHyS.

Furthermore, the additional diode for the mcHyS is a necessary component for the robust functioning of the switch, while in the tHyS of Fig. 2(b) it is added for reducing the SiC MOSFET rating, and/or to de-risk body-diode degradation during startup [22]. This diode is required to conduct the reverse current, since the SiC MOSFET is used only for the switching transitions, as possible to see from the switching pattern of Fig. 3. It has to be noted that this extra diode must be added, otherwise the current would forcefully flow through the SiC MOSFET body diode which is not sized to withstand the high current and to use the MOSFET channel in reverse conduction would not be economical, because the chip area would need to increase. Both a Si or a SiC diode are suitable for this purpose, in this paper the mcHyS is assembled with Si diode, since there are commercially available devices already packaged together Si IGBT / Si diode. TO247 devices are used in the experimental characterization. In this way the commutation inductance loop are minimized and the two devices are properly designed and selected to be complementary. As just mentioned, the advantage of such configuration is that the SiC MOSFET can have a low current rating and so low cost, while the switching losses of the switch are greatly reduced with respect to a pure Si IGBT. Such cost-performance analysis for this mcHyS is missing from the literature, therefore the potential advantages and disadvantages and practical implementation issues of such HyS are not yet clear. These are discussed in this paper in the following sections.

III. HYBRID SWITCH ANALYTICAL MODELLING

A. Conduction Losses

Conduction losses in power semiconductors can be modelled as:

$$P_c = v \cdot I_{avg} + r \cdot I_{rms}^2, \tag{1}$$

where v stands for the pn junction barrier voltage, present in IGBTs and diodes, r for the on-state resistance of the device, and I_{avg} and I_{rms} are the average and RMS current flowing through the switch, respectively. The on-state parameters of semiconductors can be extracted by the I-V curves presented in datasheets or experimentally derived. Furthermore, they are influenced by the junction temperature, T_j, following [23]:

$$r(T_j) = r_{25°C} + tc_r (T_j - 25), \tag{2}$$

$$v(T_j) = v_{25°C} + tc_v (T_j - 25). \tag{3}$$

where v and r are the semiconductor pn junction barrier voltage and the on-state resistance, and tc_v and tc_r their respective temperature coefficients. These can be derived from the datasheet of the semiconductor, for example, the thermal coefficient of the on-state resistance:

$$tc_r = \frac{r_{Tj,max} - r_{Tj,min}}{T_{j,max} - T_{j,min}}. \tag{4}$$

where Tj, max and Tj, min indicate the maximum and minimum junction temperature. The on-state resistance of a device increases with the temperature, and so tc_r is positive, while v decreases with temperature, therefore tc_v takes negative values.

Typically, for the estimation of the conduction losses through (1), the on-state characteristics are taken at the maximum allowed operating temperature, in the range of 125-150 °C, depending on the semiconductor and packaging technologies [23]–[26]. Following this approach the losses can be accurately estimated at full power, when, with properly designed cooling system, it is expected that the junction temperature reaches its maximum level. At lower power, however, the power losses will be slightly overestimated.

In a grid-connected 2L-VSC the analytical expression of I_{avg} and I_{rms} can be found averaging the line current during a switching period according to the switch duty cycle. In case of sinusoidal PWM with one quarter zero sequence voltage injection [27], the duty cycle of the upper ($D_u(\omega)$) and bottom ($D_b(\omega)$) switch can be expressed respectively as:

$$\begin{aligned} D_u(\omega) &= \frac{1}{2} + \frac{m}{2}\sin(\omega) + \frac{m}{8}\sin(3\omega); \\ D_b(\omega) &= 1 - D_u(\omega); \end{aligned} \tag{5}$$

where m is the modulation index, and ω is the phase angle. This modulation strategy leads to an improved harmonic performance with respect to simple sinusoidal PWM and space vector modulation [27].

Considering a pure sinusoidal phase current:

$$I(\omega) = \hat{I}\sin(\omega + \varphi), \tag{6}$$

where φ is the phase shift between the fundamental line voltage and current, and $\hat{I}$ is the peak AC line current, the active switch average and RMS current can be calculated solving (7) and (8):

$$I_{avg} = \frac{1}{2\pi} \int_a^b I_c(\omega)D(\omega)d\omega, \tag{7}$$

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_a^b I_c^2(\omega)D(\omega)d\omega}, \tag{8}$$

while substituting the expression of the conducted current to I_c, the angular position of the beginning and end of the conduction period to a and b, and the switch duty cycle expression to $D(\omega)$. This approach provides accurate results

if the converter switching frequency f_s is much greater than the grid frequency f_g, the bridge-leg dead time is negligible with respect to the switching period, and the maximum current ripple within a switching period is much smaller than $\hat{I}$. Such assumptions hold in grid-connected VSCs, since f_s is in the order of kHz and an L or LCL filter, which are typically designed to strongly limit the current ripple flowing in the converter, has to be placed between the VSC and the grid, so to respect the grid connection standards. The semiconductors' current stress in single switch technology based 2L-VSC can be calculated as [28]. HyS-based VSCs, instead, require different approaches.

1) mcHyS-based 2L-VSC: The mcHyS, shown in Fig. 1, foresees the MOSFET only for switching, i.e., for chip area minimization, and the full current conduction through the Si-based devices. Therefore, the conduction losses in this HyS arrangement can be calculated as the ones of a Si IGBT based 2L-VSC. Nonetheless, as shown Fig. 1, the switching strategy can be optimized by the proper selection of the switching delays $d_1...d_4$. Therefore, if the MOSFET is turned on before the IGBT and turned off after the IGBT, in this time period, it will conduct the full current. These extra conduction losses depend on the total time in which the SiC MOSFETs conduct the full current, d_{tot}, and they can be evaluated as:

$$P_{exC-M,mcHyS} = d_{tot} f_s r_{ds,on} \hat{I}^2 \frac{8m\cos\varphi + 3\pi}{24\pi}, \quad (9)$$

where $r_{ds,on}$ is the MOSFET on-state resistance.

2) tHyS-based 2L-VSC: The tHyS intends both IGBT and MOSFET for current conduction, as presented in [10]. This hybrid switch is typically implemented paralleling Si IGBTs and SiC MOSFETs, however in this paper, a Si diode is added also in this configuration so to reduce the current stress on the SiC MOSFET in rectifier operation, which otherwise leads to a large MOSFET area and therefore the tHyS would lose its cost competitiveness. Furthermore, it is considered that the SiC MOSFET body diode does not conduct, due to its high forward voltage drop. Such an assumption is confirmed by the third quadrant operation I-V curves provided by the device manufacturer [25].

The Si devices will not conduct until the voltage across the switch, V_{on}, overcomes its pn junction barrier potential v_{pn}, that is $v_{ce,0}$ in the case of the IGBT and $v_{f,0}$ in the case of the diode. Therefore, the current values over which the bipolar devices starts conducting and their angular position are defined as:

$$I^* = \frac{v_{pn}}{r_{ds,on}}, \quad (10)$$

$$\delta^* = \arcsin\left(\frac{v_{pn}}{r_{ds,on} \cdot \hat{I}}\right). \quad (11)$$

The Si IGBT conducts in the angular interval $\omega \in [\delta - \varphi ; \pi - \delta - \varphi]$ and the diode during the interval $\omega \in [\pi + \delta_r - \varphi ; 2\pi - \delta_r - \varphi]$, where δ and δ_r are found substituting respectively the IGBT and diode on-state parameters in (11).

For line current values, $I(\omega)$, larger than I_f^* and lower than I_r^* the current sharing between Si devices and MOSFET can be derived according to the devices on-state characteristics, as:

$$I_{M,f}(\omega) = \frac{I(\omega)r_{ce} + v_{ce,0}}{r_{ds,on} + r_{ce}}, \quad (12)$$

$$I_I(\omega) = \frac{I(\omega)r_{ds,on} - v_{ce,0}}{r_{ds,on} + r_{ce}}, \quad (13)$$

$$I_{M,r}(\omega) = \frac{I(\omega)r_f + v_f}{r_{ds,on} + r_f}, \quad (14)$$

$$I_d(\omega) = \frac{I(\omega)r_{ds,on} - v_f}{r_{ds,on} + r_f}, \quad (15)$$

where r_{ce} and r_f are the on-state resistance of the Si IGBT and Si diode respectively. Equations (12) and (13) are referred to the forward conduction stage of the switch, while (14) and (15) to the reverse conduction stage. Overall, the tHyS on-state characteristics can be expressed as:

$$V_{on,tHyS}(I) = \begin{cases} r_{ds,on} \cdot I_{M,r} & \text{if } I <= I_r^* \\ r_{ds,on} \cdot I & \text{if } I_r^* < I < I_f^* \\ r_{ds,on} \cdot I_M & \text{if } I >= I_f^*. \end{cases} \quad (16)$$

The average and RMS current flowing through the IGBT can then be calculated substituting $I_I(\omega)$ in (7)-(8) and integrating during its conduction interval:

$$I_{avg,I} = \frac{1}{2\pi} \int_{\delta-\varphi}^{\pi-\delta-\varphi} I_I(\omega) D_u(\omega) d\omega, \quad (17)$$

$$I_{rms,I} = \sqrt{\frac{1}{2\pi} \int_{\delta-\varphi}^{\pi-\delta-\varphi} I_I^2(\omega) D_u(\omega) d\omega}. \quad (18)$$

Similarly, the diode current stress can be found as:

$$I_{avg,d} = \frac{1}{2\pi} \int_{\pi+\delta_r-\varphi}^{2\pi-\delta_r-\varphi} I_d(\omega) D_u(\omega) d\omega, \quad (19)$$

$$I_{rms,d} = \sqrt{\frac{1}{2\pi} \int_{\pi+\delta_r-\varphi}^{2\pi-\delta_r-\varphi} I_d^2(\omega) D_u(\omega) d\omega}. \quad (20)$$

It has to be noted that for peak AC current lower than the minimum current necessary for the IGBT to conduct, the value of δ becomes equal to $\pi/2$, and therefore the integration interval in (17)-(20) becomes null. The conduction losses are then fully flowing across the SiC MOSFET.

As previously mentioned, the MOSFET conducts during the full period, however when the bipolar devices are conducting the MOSFET sees only a fraction of the total current. The rms current flowing through it is then found according to:

$$I_{ms,M} = \left(\frac{1}{2\pi} \left(\int_{\delta-\varphi}^{\pi-\delta-\varphi} I_M^2(\omega) D_u(\omega) d\omega + \right. \right.$$
$$\int_{\pi-\delta-\varphi}^{\pi+\delta_r-\varphi} I^2(\omega) D_u(\omega) d\omega + \int_{\pi+\delta_r-\varphi}^{2\pi-\delta_r-\varphi} I_{M,r}^2(\omega) D_u(\omega) d\omega$$
$$\left. \left. + \int_{2\pi-\delta_r-\varphi}^{2\pi+\delta-\varphi} I^2(\omega) D_u(\omega) d\omega \right) \right). \quad (21)$$

TABLE I
VALIDATION OF THE EQUATIONS PROPOSED IN SECTION III-A THROUGH
THE CIRCUIT SIMULATOR PLECS

		Analytical calculation	Simulation	Error %
mcHyS	$I_{\mathrm{avg,T}}$	51.01	49.78	+2.41
	$I_{\mathrm{avg,D}}$	13.97	14.09	-0.85
	$I_{\mathrm{rms,T}}$	90.87	89.14	+1.90
	$I_{\mathrm{rms,D}}$	46.48	46.08	+0.86
tHyS	$I_{\mathrm{rms,M}}$	42.94	42.50	+1.02
	$I_{\mathrm{avg,T}}$	28.51	28.23	+0.98
	$I_{\mathrm{rms,T}}$	52.27	51.40	+1.66
	$I_{\mathrm{avg,D}}$	8.06	8.11	-0.62
	$I_{\mathrm{rms,D}}$	28.50	28.27	+0.81

Additionally, the extra conduction losses in the MOSFET due to the turn on and off delay would then only happen for current levels higher than I^*, since for lower current the MOSFET would conduct the full current anyway. These can then be estimated by:

$$P_{\mathrm{exC-M,tHyS}} = \frac{r_{\mathrm{ds,on}}d_{\mathrm{tot}}f_s\hat{I}^2}{24\pi}\Big[6(2m + \sin\delta)\cos\delta - 4m\cos^3\delta + 3(\pi - 2\delta)\Big]. \quad (22)$$

3) Current stress equations verification through circuit simulator: The accuracy of the proposed equations is verified with the circuit simulation software PLECS.

A simulation model of a 2L-VSC assembled with different switch technologies has been built so to calculate the average and RMS current flowing through the different components of the HySs at different operating points. The simulation parameters considered are f_s=10 kHz, V_{dc}=900 V, $V_{\mathrm{ac,ll}}$=400 V, P_n=100 kW, and φ=0.

The 2L-VSC is interfaced with the grid through a filter inductance with a value of 1 mH, thus resulting in a low current ripple, below 1% the peak AC current. For the verification of the HySs arrangements, $v_{\mathrm{ce,0}}$ and $v_{\mathrm{f,0}}$ are set to 0.9V and 1V respectively. The on-state resistances considered are r_{ce}= 20 mΩ, $r_{\mathrm{ds,on}}$= 40 mΩ, and r_{f}= 15 mΩ. These values are compatible with the I-V characteristics of the devices considered in the next section's experimental testing. The simulations are run with a variable step solver, DOPRI (non-stiff), with maximum step size and relative tolerance of 1μs.

Table I displays the average and RMS current values flowing through a single switch of a 2L-VSC operated as a full-power factor inverter calculated through the analytical method presented in this Section and the PLECS model. It can be noted that the analytical expressions provide excellent accuracy with respect to the circuit simulations.

B. Switching losses

The switching losses of a 2L-VSC can be analytically calculated through the following general equation:

$$P_s = \frac{f_s}{2\pi}\int_0^{2\pi} E_{\mathrm{sw}}(V_{\mathrm{dc,sw}}, I(\omega))\mathrm{d}\omega. \quad (23)$$

where E_{sw} represents the device switching energy as function of the switched voltage $V_{\mathrm{dc,sw}}$ and current I. The voltage dependence can be considered linear, while the current dependence can be approximated by quadratic functions. This approach is valid for 2L-VSCs, regardless on the switch configuration. E_{sw}, instead, is characteristic of each device, and, for HySs, it is also influenced by the switching delays $d_1...d_4$, as it is discussed in Section IV.

IV. EXPERIMENTAL CHARACTERIZATION

The conduction and switching performances are characterized through single and double pulse tests (SPT and DPT) whose circuit schematics are illustrated in Fig. 4(a)-(b), together with the thermal conditioning circuit in Fig. 4(c). The tests have been carried out with four devices in parallel with a common external gate resistor, R_g of 4 Ω and gate driver voltages, $V_{\mathrm{gs}}, V_{\mathrm{ge}}$ for MOSFET and IGBT respectively, of +17/-4 V. In order to control the temperature of the device under test, a heating resistor MP9100-100 and an NTC thermistor TO-103J2F are attached to the semiconductors' heatsink. The thermal circuit for the control and monitoring of the semiconductor case temperature is shown in Fig. 4(c). Additionally, during the tests, a FLIR thermal camera is used to ensure that the temperature is within the test range. The semiconductors under tests are the 1200 V class SCT3040KL SiC MOSFET manufactured by Rohm Semiconductor [25], and the IKQ40N120CT2 Si IGBT/diode manufactured by Infineon [24], both rated for 40 A. The choice of discrete TO-247 semiconductors for the HyS testing is driven by the necessity of minimizing the commutation loops between the switches which are detrimental for the switching performances. In this context, the paralleling of modules would require significantly larger connections between the individual components, due to their larger size compared to discrete TO-247 devices. Ideally, commercial HyS could be assembled with both Si and SiC devices inside the same power module, to further reduce stray inductances and ensure optimal performances.

The tests are carried with four devices in parallel to constitute a single switch, resulting in a 160 A switch, therefore the HySs are assembled with the hard-paralleling of two SiC MOSFETs and two Si IGBTs. The PCB layout aims at minimizing the parasitic inductances between the switches, placing them close to each other, so that they would properly share the dynamic current. A perfect current sharing during the switching transitions between the parallel devices can be ensured only by employing properly tuned separate gate driver for each device. This solution increases the complexity and cost of the system. Alternatively, one gate driver for each switch technology can be used, resulting in a good trade-off between optimal current sharing and system complexity. In this way the switching transitions are properly coordinated between the SiC-MOSFETs and the Si-IGBTs. Nonetheless, it is not guaranteed that the two SiC-MOSFETs exactly share the current during the switching transitions. In this context the PCB layout and minimization of parasitic inductances is crucial to ensure the best performances.

The experimental implementation of the double pulse tester is shown in Fig. 5(a), together with (b) the
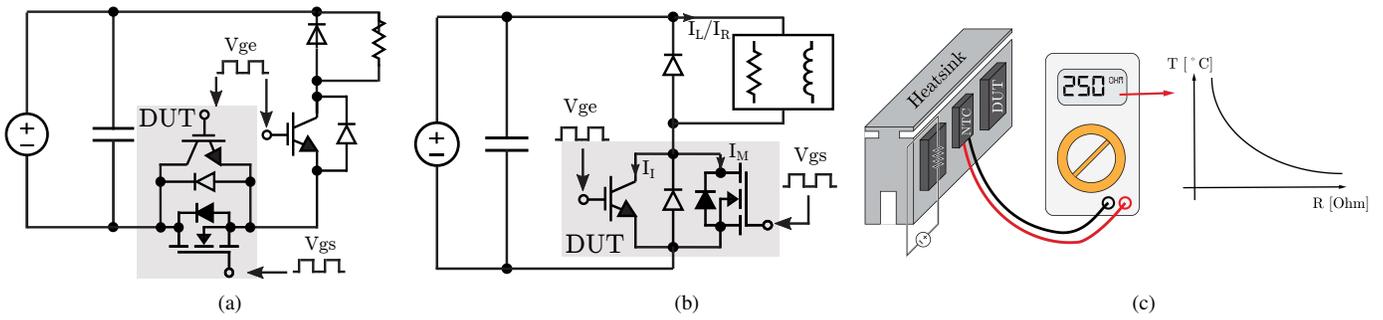
Fig. 4. Electrical circuit schematics for the experimental derivation of (a) the reverse conduction characteristics of various switches, and of (b) the forward conduction and switching characteristics, and (c) thermal circuit for the control and monitoring of the semiconductor case temperature.
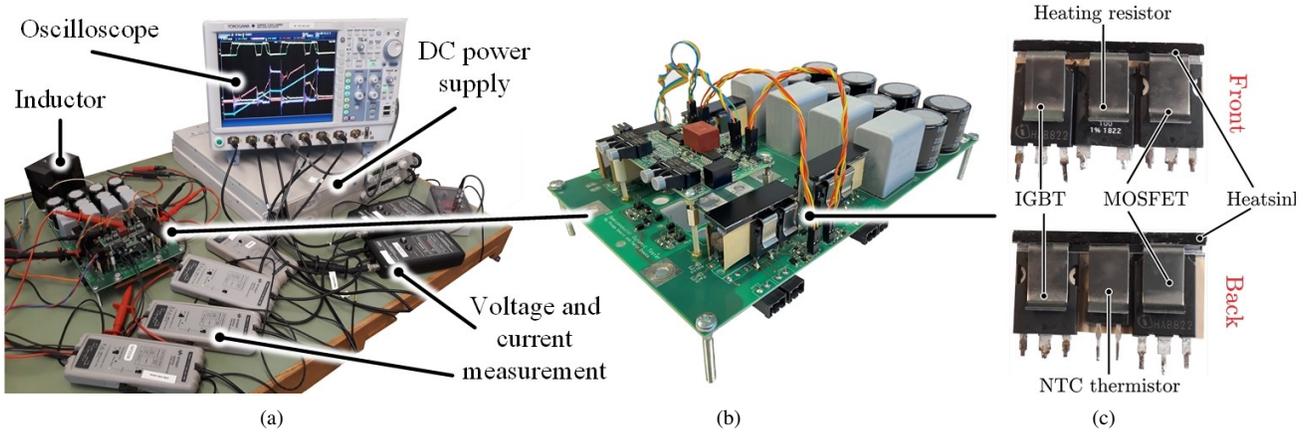

Fig. 5. (a) Test set up, (b) DPT board with gate driver on top, and (c) semiconductors and thermal management devices for the characterization of the semiconductors devices.

semiconductor board and its gate driver, and (c) the thermal management devices and their arrangement together with the semiconductors.

1) Conduction Losses: The forward conduction losses are evaluated through a resistive SPT where a resistive load is connected in parallel to a diode and a short pulse is sent to the bottom switch [Fig 4(b)]. The pulse width is selected to be 15 μs, to limit self-heating, but long enough to compensate the parasitic circuit voltage drops. For the reverse conduction characteristics the circuit is slightly modified and the device under tests is connected between a switch and the DC capacitors with the emitter/source connected with the emitter of the switch [Fig 4(a)]. A low DC voltage, in the range of 5-20 V, is impressed across the half-bridge so that low voltage probes can be used for measuring the voltage drop over the switch, guaranteeing higher accuracy, since the voltage across the switch under test is in the order of few volts.

The forward and reverse on-state characteristics of the single technology switches are shown in Fig. 6 (a)-(b) together with the one of the HySs. Comparing the tHyS's conduction I-V curves with the IGBT and MOSFET ones [Fig. 6 (a)-(b)] it can be seen that for low current level, such as below 50 A, the tHyS would perform significantly better than the IGBT and mcHyS solution, very close to the MOSFET curve. In this context, the tHyS becomes attractive for applications that require frequent operation at low partial loads. Furthermore, at
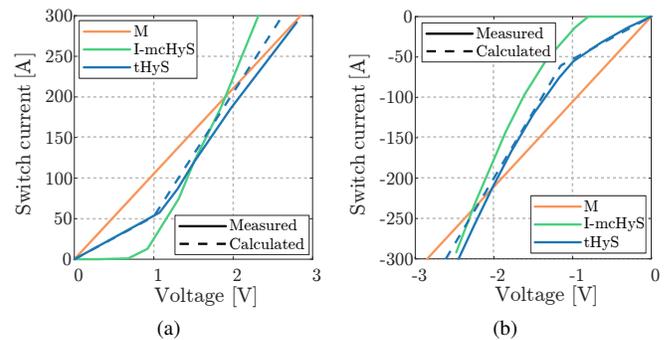

Fig. 6. Forward (a) and reverse (b) on-state characteristics of four parallel SiC MOSFET, four parallel Si IGBT, and two Si IGBT plus two SiC MOSFET in parallel, derived for T_j=25° C, V_{gs} and V_{ge}=+17/-4 V, and R_g=4Ω, and analytically calculated according to (16).

a high current level ($>$250 A) this hybrid solution starts having better conduction performances than the MOSFETs, but worse than the IGBT and mcHyS. It has to be noted that the mcHyS follows the Si IGBT-diode I-V curve, since the SiC MOSFET is activated only during the switching transitions. Therefore, only the tHyS shows an improved conduction characteristic with respect to the IGBT solution.

Together with the HyS I-V curve, the current sharing between IGBT/diode and MOSFET is a crucial information for the design and optimization of the HyS and its components. The current sharing at different total switch current with
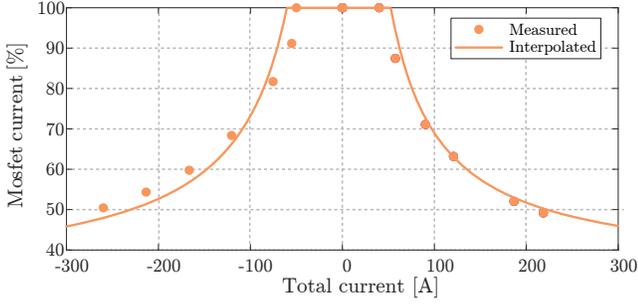
Fig. 7. Percentage of the total conducted current by the tHyS flowing through the MOSFET channel; derived for T_j=25° C, V_{gs} and V_{ge}=+17/-4 V, and R_g=4Ω, and analytically calculated according to (12) and (14).
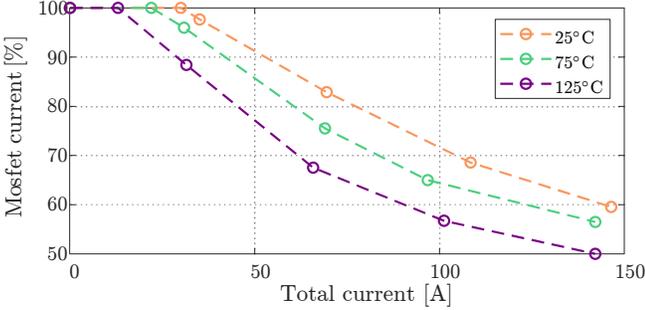

Fig. 8. Measured current flowing through the MOSFET in a HyS at different junction temperatures; derived for V_{gs} and V_{ge}=+17/-4 V, and R_g=4Ω

T_j=25° C, V_{gs}=17/-4 V and V_{ge}=17/-4 V is shown in Fig. 7. As described in Section III, the junction temperature influence the on-state parameters of the switches, and therefore the current sharing in the hybrid switch [29]. The resistance of the MOSFET channel increases with the rise in temperature, on the other hand, the pn junction barrier voltage of the IGBT decreases. In consequence, the starting value for the conduction of the IGBT is lower at higher temperature and overall the MOSFET will conduct a lower percentage of the total current, due to the higher on-state resistance. This trend is shown in Fig. 8 where the percentage of current flowing through the MOSFETs of the tHyS are measured at various junction temperatures, between 25°C and 125°C, which is the temperature range in which power semiconductor typically operate. The difference in current sharing is significant for a high temperature swing, as shown in Fig. 8. During the switching transition and the 50Hz cycles, instead, the temperature rise is smaller, due to the lower time constants, and so the current sharing is not significantly influenced by such fast temperature swings [30], [31].

The HyS I-V curves and the IGBT/MOSFET current sharing can be analytically derived as presented in Section III from the single component's on-state characteristic and (12)-(15). The analytically calculated and the experimentally measured I-V curves and current sharing are compared in Fig. 6 and Fig. 7, where it can be seen that the analytical equations provide a fair accuracy.

2) Switching Losses: The switching performances are characterized by inductive DPT, as illustrated in Fig. 4(a). Various tests have been performed, investigating the effect of
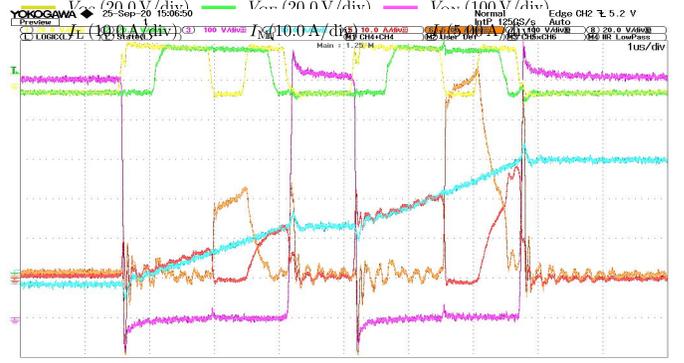

Fig. 9. Double Pulse Test waveforms of mcHyS obtained through the test setup of Fig. 5 and referred to the circuit schematic of Fig.4 (a).

temperature, turn on and off delays, and the losses sharing between IGBTs and MOSFETs in the HySs. The DC voltage V_{dc} is kept to 600 V, while different current points are achieved varying the inductance value and the pulse width. An example of the DPT waveform for the alternative HyS is shown in Fig. 9. After the deskew of the measurement probes the switching losses can then be calculated by multiplying the voltage and current waveforms during the switching event, as detailed in the datasheets of the components [24], [25].

The turn on and off delays, d_1 and d_4, have been proved in previous literature to strongly influence the switching performances of HySs. At the turn on, a small or even null delay between MOSFET and IGBT leads to minimized overall turn-on losses since both devices offer a path for the reverse recovery current and therefore shortens the turn-on time and reduces losses. This trend is also confirmed in the performed experiments, as possible to see in Fig.10(a). Regarding the turn-off, instead, a longer delay, in the range of 1-2 μs, is found to be the most suitable to reduce the turn off losses, as shown in Fig.10(b). This comes from the fact that a long delay allows the IGBT to be switched off with ZVS. However, after switching off the IGBT, the MOSFET conducts the full current, creating additional conduction losses. Therefore, long turn-off delays are penalized from these additional conduction losses, and so the optimal turn-off delay, for the considered components, has been found to be equal to 1.5 μs, a value compatible with the one reported in other studies [32]. In these conditions, simultaneous turn-on and 1.5 μs delay for turn-off, the switching losses are concentrated in the MOSFETs, with the IGBT operated in soft-switching. After all, HySs position themselves very well when compared with single technology Si and SiC switches, as indicated in Fig. 11. Both HySs can significantly reduce switching losses with respect to Si IGBTs; however, full SiC MOSFETs still exhibits the best switching performances.

3) Parasitic inductance effect in the mcHyS: The mcHyS concept, presented in Fig. 1, requires two additional switching events, defined by d_2 and d_3. These have been tested to be lossless since they happen when the switch is already conducting, and therefore, the voltage across the switch is in the order of few Volts, as it can be seen in Fig.9. This soft-switching condition is maintained when the parasitic
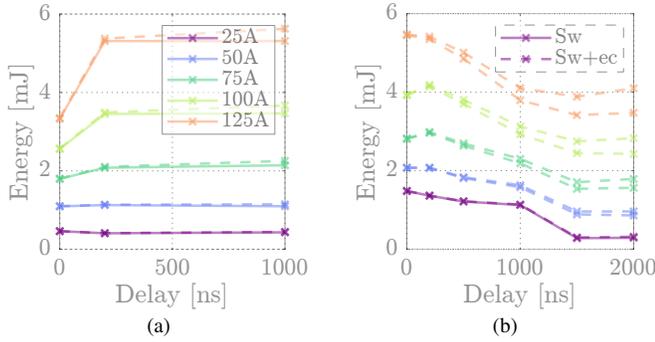
Fig. 10. HySs turn on (a) and off (b) switching energies (sw) and extra conduction (ec) losses varying the switched current and the MOSFET-IGBT delays d_1 and d_4.
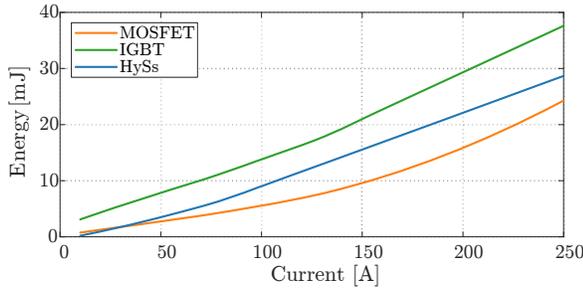

Fig. 11. Switching characteristics of HySs and Si IGBTs and SiC MOSFETs derived through DPT at T_j=25° C, V_{dc}=600 V, R_g=4Ω.
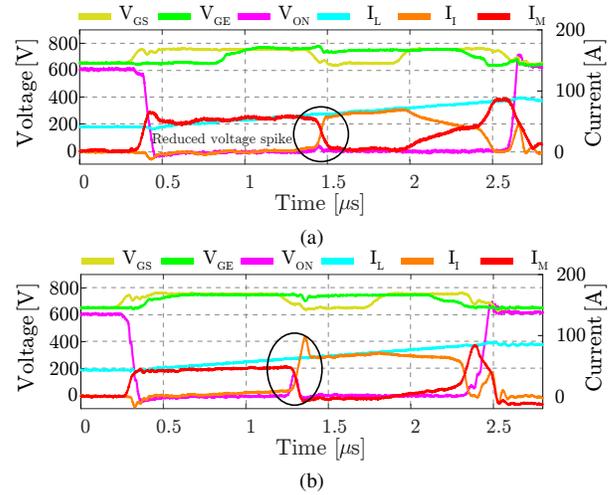

Fig. 12. Experimental verification of the influence of parasitic inductance on switching behaviour of hybrid switches: (a) low inductive commutation path, estimated to 50 nH, and (b) high inductive commutation path, estimated to 140 nH.
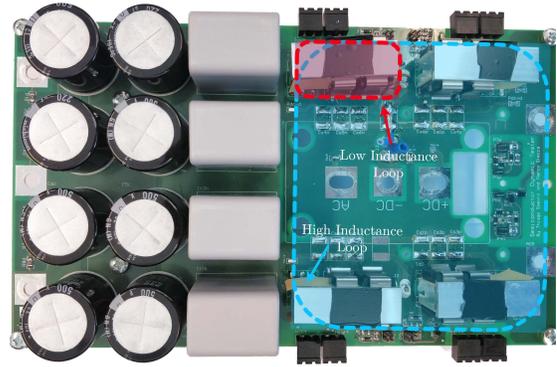

Fig. 13. Large (blue) and low (red) inductance commutation loops between parallel switches in the experimental prototype.

inductance between MOSFET and IGBT is very low so that the current commutation between the two switches occurs smoothly, as can be seen in Fig. 12 (a), where the commutation inductance of the testing setup, indicated by the red area in Fig. 13, is estimated to be 50 nH. However, if the commutation inductance is increased, the voltage across this can force the conduction of the upper diode and the rise of the voltage across the switch, as possible to see in Fig. 12 (b), where the commutation inductance of the setup, indicated by the blue area in Fig. 13, is increased to 140 nH. This voltage spike introduces additional switching losses. Therefore a low inductive commutation path between the SiC MOSFET and Si IGBT is fundamental in HySs. Furthermore, no influence of d_2 on the switch turn on losses, dependant instead on d_1, has been found. Hence d_2 and d_3 can be set very small so to avoid extra conduction losses in the MOSFETs.

4) Common-mode EMI: The conductive EMI of a grid connected converter is related to the switched terminal voltages amplitude and to switching transitions where the dv/dt is particularly relevant for common-mode EMI. The switch terminal voltage amplitude is defined by V_{dc} and the selected circuit topology. Therefore, the main switching transitions and the amplitude of the terminal voltages will be defined by the circuit topology. Regarding the dv/dt of the terminal voltages, as shown in Fig. 9 and 12, only the first and last switching events of the SiC MOSFET in a mcHyS have influence in the voltage across the switch and the equivalent terminal voltage, since the other switching transitions within the pulse period are functional switching events so to shift the current conduction from the SiC MOSFET to the Si IGBT

and vice-versa. Therefore, the voltage across the switch is driven by the first turn on and the last turn off of the SiC MOSFET, and so the dv/dt at the mcHyS output terminals is driven by the switching speed of its SiC MOSFET. Hence, the mcHyS shows similar performances of the pure SiC MOSFET solution. Overall, the pure Si IGBT solution is the one with lower high frequency common mode noise, due to the slower switching transitions [33].

5) Efficiency testing of a 10kW 2L-VSC: After the experimental characterization of the mcHyS, its efficiency has been benchmarked versus pure technology switches when implemented in a 10kW three phases 2L-VSC operating as inverter supplying a resistive load. The circuit schematic of the 2L-VSC is illustrated in Fig. 14. The 10kW 2L-VSC prototype is shown in Fig. 15, with at the bottom the output LCL filter used to interface the VSC with the resistive load. This 10 kW VSC could be used as a Power Electronic Building Block (PEBB) for a 100kW unit, however here the VSC is optimized only for verifying the advantage of the system in the 2L-VSC inverter application. Nonetheless, the performances should be similar in terms of efficiency.

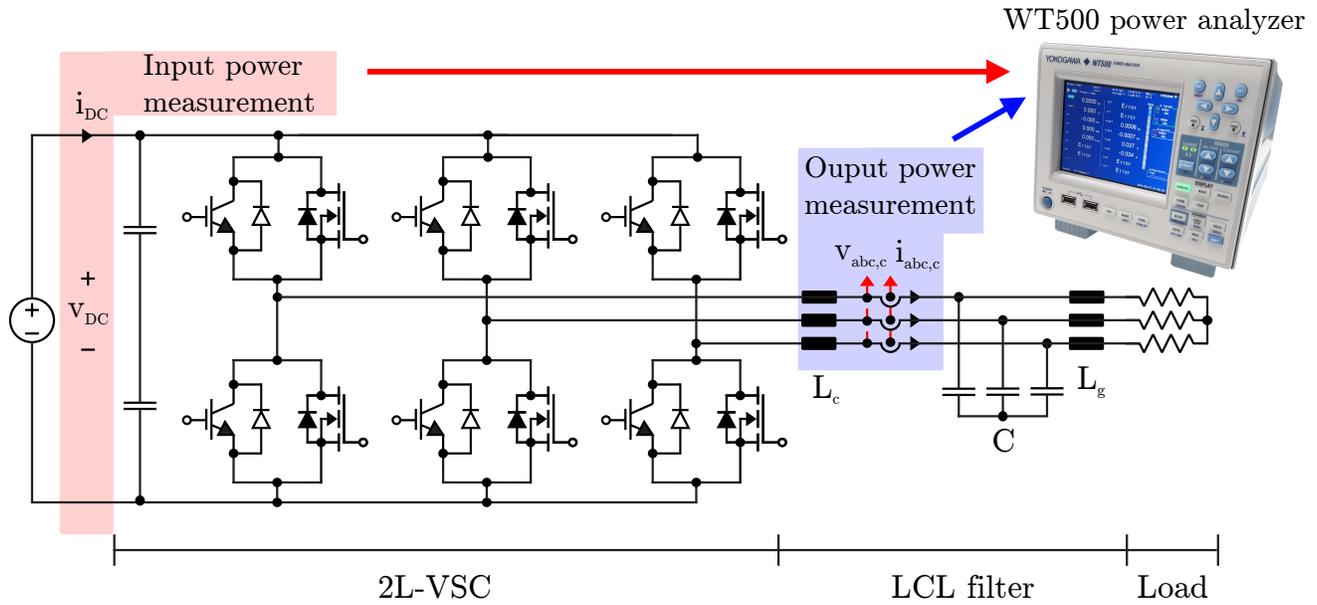The mcHyS switching waveform during the inverter

Fig. 14. Circuit schematic of a 2L-VSC operating as inverter supplying a resistive load. The connection points for the efficiency measurements through the WT500 power analyzer are highlighted.

Fig. 15. Prototype of the 10kW 2L-VSC used for the efficiency testing of the mcHyS with LCL filter in the bottom.
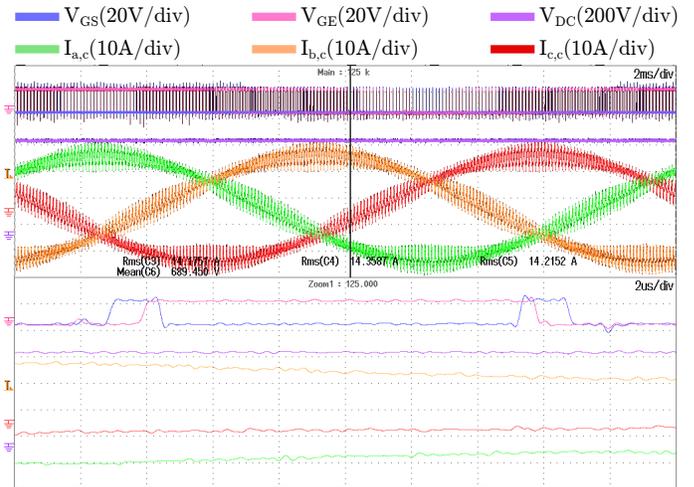

Fig. 16. Waveforms of a mcHyS-based 2L-VSC supplying a resistive load. The switching pattern of the mcHyS can be distinguished in the zoomed bottom area of the figure, the gate signals of the SiC-MOSFET and of the Si-IGBT are shown with the blue and pink waveform respectively.

operation at 10kW is shown in Fig. 16, where the VSC three phases converter side output currents are indicated with the green, orange and red waveforms, and the gate signals of the mcHyS MOSFET and IGBT with the blue and pink signals. The modulation pattern of Fig. 1 can be recognized in the zoomed lower part of Fig. 16. Furthermore, the DC voltage waveform is displayed with purple color.

Three different switch configurations have been benchmarked: two pure switch technologies, the Si-IGBT and SiC-MOSFET; and the mcHyS. The switches are selected to have comparable rated continuous collector/drain current at 100 °C. The IKQ40N120CH3 Si-IGBT, rated for 40 A, from Infineon has been selected. Two SCT3105KL SiC MOSFETs,

rated 17 A, from Rohm Semiconductors have been paralleled to assemble the SiC-based switch. Finally, the mcHyS, has been set up paralleling a IKQ40N120CH3 Si-IGBT, rated for 40 A, and one SCT3105KL SiC MOSFETs, rated for 17 A. Considering the cost figures from components distributors, the costs of a single switch are compared in Table II [34]. It can be seen that the pure SiC-MOSFET solution is nearly four times more expensive than the pure Si-IGBT, while, the mcHyS provides a trade-off solution, with triple the IGBT price.

The efficiency tests have been performed with an input DC voltage of 685 V, an output AC rms voltage of 230 V, modulation index of 0.95, and 10 kHz switching frequency. An LCL filter is placed between the VSC and the load

Parameter	Si-IGBT	mcHyS	SiC-MOSFET
Single switch cost [€]	5.53	16.48	21.90
Cost ratio to Si-IGBT [p.u.]	1	2.98	3.96
2L-VSC efficiency at 10kW [%]	98.19	98.56	99.00
Loss reduction to Si-IGBT [%]	-	-37.45	-83.23

resistors, to filter the current harmonics, as required by the grid connection standards. The LCL filter is assembled with the commercially available 750343810 inductors from Wurth Electronics rated 340mH both in the converter and in the grid side, L_c and L_g, and 9.9 uF capacitance, C. The efficiency, evaluated through the Yokogawa WT500 Power Analyzer, has been measured between the DC side of the VSC and the converter side inductance of the LCL filter, L_c. In this way, both the losses of the 2L-VSC and of L_c are measured. The power analyzer connection after L_c has been selected to ensure that the efficiency measurement has high accuracy, since the switched voltage at the output of the VSC has very high dv/dt and cannot be properly measured by the power analyzer, while after L_c the voltage has a more sinusoidal shape with much lower dv/dt than the WT500 power analyzer can accurately measure. In Fig. 17(a) the measured efficiency of the three switch configuration in five operating points are shown. Additionally, the losses in the converter side inductors are calculated evaluating the AC winding losses, proximity effect losses and core losses through the methods described in [35]. The AC and DC resistance has been measured through the Agilent 4294a Impedance Analyzer, while the Steinmetz parameters are derived from the datasheet of the inductor's core material. The calculated inductor efficiency for different power flowing through it is also shown in Fig. 17(a).

Finally, given the measured efficiency of the set up of Fig. 14, VSC+L_c, and the calculated losses of L_c, it is possible to provide a close estimate of the semiconductors efficiency, plotted in Fig. 17. The pure SiC MOSFET switch, as expected, provides the most efficient solution. Furthermore, the efficiency gain of mcHyS with respect to the pure Si-IGBT is remarkable, positioning itself as good trade-off between Si-IGBT and SiC-MOSFET. As summarized in Table II, the mcHyS allows a 37.45% reduction of power losses respect to the IGBT at 10kW.

V. CHIP AREA AND COST OPTIMIZATION

In HySs the current ratio between the SiC MOSFET and Si IGBT defines not only the current sharing behavior, and thus the performance of the switch, but also its cost. A low current ratio, in fact, would result in a small SiC chip area and, therefore, lower switch costs since the silicon carbide devices are by far more expensive than their silicon based equivalents. However, a small chip area leads to worse conduction and thermal performances. On the other hand, a too high current ratio could result in over dimensioning the SiC area and thus loses cost-competitiveness versus the full Si IGBT based switches. In this context, optimizing the Si and SiC chip area ensures that both technologies are properly
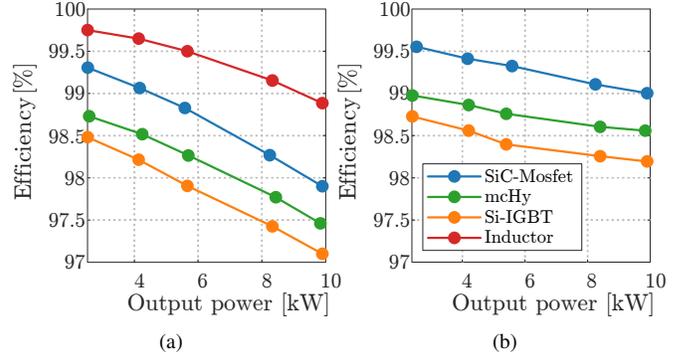

Fig. 17. (a) Measured efficiency of a 10kW 2L-VSC and of the converter side inductor, assembled with different switch technologies, and calculated efficiency of the inductor at various power, and (b) derived VSC efficiency.
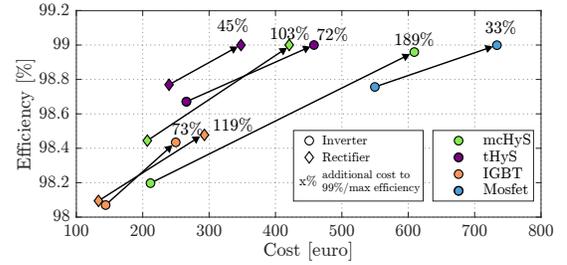

Fig. 18. Semiconductor chip costs and efficiency design space for different switch configuration that satisfy the thermal limits during operation at full power in an 2L-VSC working as inverter and rectifier. The percentage shown is related to the incremental cost needed to bring the minimum cost designs to an efficiency of 99% or to the maximum efficiency.

utilized and that the switch cost is optimized [12]. The chip area optimization consists of finding the minimum necessary Si and SiC chip area of each switch so that the semiconductors' thermal limitations are not exceeded, which means a maximum junction temperature of 150°C.

Therefore, in this section, the semiconductor chip area optimization of a grid-connected 100 kW 2L-VSC is presented. A low line-to-line AC voltage, $V_{ac,ll}$, of 400 V, a DC-link voltage, V_{dc}, of 900 V, and a switching frequency, f_s, of 10 kHz are considered. The analysis here presented is based on the analytical equations provided in Section III, on the experimentally derived switching energies, as illustrated in Section IV, on datasheet values from semiconductor manufacturers [24]–[26], and on the cost figures from components distributors [34].

Power semiconductors on-state resistance r_{on} and junction to case thermal resistance $R_{th,jc}$ are generally modelled following an inverse correlation with the chip area A_c, as [36], [37]:

$$r_{on} = \frac{x}{A_c} \quad (24)$$

$$R_{th,jc} = M \cdot A_c^{-l}. \quad (25)$$

The pn junction barrier voltage of IGBTs and diodes instead depends on its manufacturing technology, not on the device chip area.

The switching losses and chip area can be correlated with piecewise linear functions as a function of the switched

TABLE III

	Parameter		Si IGBT	Si diode	SiC MOSFET
Chip area	A_i	mm^2	20-70	10-60	2-20
Conduction	x_i	mΩ/mm^2	723	233	357.3
	V_{ce}	V	0.9	1.05	-
Turn on/[1]	$m_{s,i}$	mJ/mm^2	-0.134	0.0814	-0.058
Reverse Rec[1]	$q_{s,i}$	mJ	11.29	1.7456	1.945
Turn off[1]	$m_{s,i}$	mJ/mm^2	0.018	-	-0.033
	$q_{s,i}$	mJ	2.977	-	0.882
Thermal	M_i	-	6.558	3.022	1.585
	l_i	-	0.826	0.491	0.705
Cost[2]	$m_{c,i}$	€/mm^2	0.2	0.15	4.256
	$q_{c,i}$	€	2.846	0.827	-5.264

[1] at 50A/600V.
[2] for Si IGBT and Si diode referred to bare dies, while for SiC MOSFET to TO-247 packaged, subtracting the packaging cost (cf. [38]), due to the unavailability of bare die cost information.
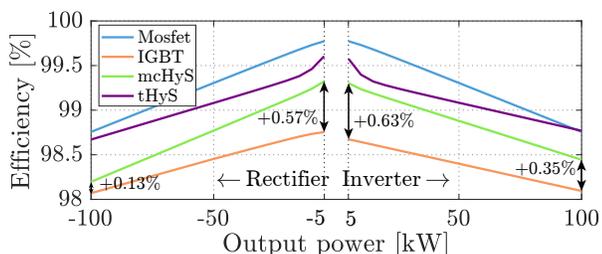

Fig. 19. Semiconductor efficiency of the switch configurations of Fig. 19 varying the output power operating as inverter and rectifier 2L-VSCs. The selected designs are shown in Fig. 18 and represent the chip area optimized for minimal cost.
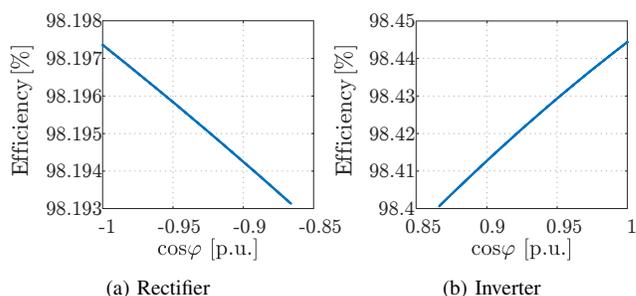

(a) Rectifier (b) Inverter

Fig. 20. Semiconductor efficiency of a mcHyS-based 2L-VSC designed as (a) inverter and (b) rectifier operating at rated apparent power and varying the power factor.
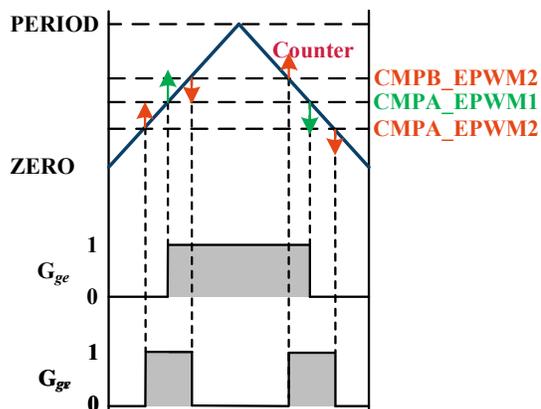

Fig. 21. Implementation of the mcHyS PWM in a digital controlled.

current. However, to provide a fair chip area analysis, it has to be considered that generally larger chips are switched faster through smaller gate resistances [24], [37], [39], [40]. Therefore the switching losses are first to be scaled to have a fixed value of gate resistance per mm^2 of semiconductor area, according to the suggested values from the manufacturers, and then interpolated. The switching losses relation with chip area can then be modelled as:

$$E_{sw}(A_c, I, V) = m_s(I, V) \cdot A_c + q_s(I, V). \quad (26)$$

In addition to the performance indicators, the semiconductor cost can be expressed proportionally to its chip area and linearized in the form of:

$$C = m_c \cdot A_c + q_c. \quad (27)$$

The fitting coefficients of (24)-(27), listed in Table III, have been derived consulting the manufacturer's datasheet, the components distributors prices, and the experimentally derived results presented in Section IV.

The minimum cost chip area configurations are then calculated for a 2L-VSC, IGBT-based, MOSFET-based, and HyS-based, designed to operate as an inverter, or rectifier. The operation mode influences the conduction losses, e.g. the rectifier mode leads to a higher reverse conduction current in the switches. These are plotted versus their efficiency in Fig. 18, where it can be noted that the IGBT based

switch, as expected, provides the cheapest solution in both operating modes. In the same figure the designs that reach 99% semiconductor efficiency or, in the case of the IGBT, the maximum efficiency designs, are also plotted, so to show the required cost increase to reach such efficiency value. The mcHyS minimum cost solution shows relatively low costs compared to its full SiC MOSFETs equivalent. The tHyS still provides a cheaper solution than the pure SiC MOSFET one, however, since the SiC MOSFET is also used for conduction it requires a larger area than in the mcHyS and thus becomes more expensive. For high efficiency designs, $\eta \geq 99$ %, the tHyS shows low costs, lower than mcHyS and full SiC MOSFETs. Furthermore, in Fig. 19, the minimum cost configurations' efficiency is plotted for various power outputs. Overall, at low power the efficiency gain of HySs and MOSFETs versus the IGBT-based solution is remarkable, with an efficiency gain of the mcHyS of up to 0.6% with respect to the IGBT. Grid connection standards typically require VSC to support the grid voltage with reactive power, therefore it is important to consider the standard required power factor, typically 0.9, in the VSC design [41]–[43]. In Fig. 20, the efficiencies of mcHyS-based 2L-VSCs designed as inverter and rectifier are shown varying the power factor when operating at rated apparent power. It can be seen that the efficiency drops slightly when more reactive power is generated, nonetheless it remains satisfactory.

In this Section the semiconductor costs of various switch technologies have been considered. Nevertheless, the

semiconductor die are not the only cost factor. Other elements are, for example, the packaging, gate driving and protection circuit, and digital controller cost.

A fixed cost disadvantage of HySs versus the pure technologies is found on the gate driving circuits. Such switch assembly, in fact, requires two separate gate driving circuit per single switch, since the Si-IGBT and SiC-MOSFET are controlled separately, as Fig. 1 details. Nonetheless, commercial dual channel digital isolators can be purchase with similar costs than their single channel counterparts, i.e. the ADUM1100 and ADUM1200 serie. Therefore the extra costs in the dual channel gate driver of the mcHyS consists on the two buffers required instead of one, which are a relatively cheap component, i.e. the ZXMC4559DN8. Regarding all the remaining previously mentioned elements, the HySs do not require higher fixed costs or significantly higher complexity. Packaging costs can be assumed to be constant between the switch technologies. Current implementation of HySs are based on paralleling separate discrete Si and SiC based devices [17], [19], therefore there is not an added packaging costs for HySs with respect to single technology switches. Furthermore, also if packaged in a power module there would not be significantly different packaging costs, since multi device packaging technology is already mature, as most high power semiconductors module are assembled with multiple dies in parallel [23]. This is particularly true in case where the die attachment and bond-wiring technologies can be the same for both Si and SiC, e. g., similar die sizes.

The protection of the switch can be ensured through several ways, depending on the switch short circuit withstanding time. Si-IGBT generally can withstand short circuits for longer time, up to 8-10 μs, therefore, the desaturation method, implemented in the gate driver, is the most commonly used protection systems [44]. SiC-MOSFETs, instead, require a faster clearing time, in the order of 1-2 μs, which is quite challenging to achieve through the desaturation method. Therefore, other protection system have been studied, such as di/dt measurement through Rogowski coils or direct switch current measurement [44], [45]. In this context, HyS have the same requirements of the pure SiC counterparts.

The digital controller which is typically used for generating the PWM signals of the converter with single switch can be used also for the control of HySs-based converters. The gate signals, in fact, are typically generated through a counter compare technique, i.e., by comparing a value, which defines the switch duty cycle and varies each switching period, with a triangular carrier. In the same way, the gate signals strategies of a HyS can be generated, using an additional counter compare, shifted from the first counter compare accordingly to the delays between the IGBT and MOSFETs switching transitions. The implementation of the mcHyS PWM pattern in a TI μcontroller is shown in Fig. 21, where it can be seen how using two counter compares the modulation signal of the mcHyS can be generated in the high resolution PWM module.

VI. APPLICATIONS IN VSCs

The particular characteristics of HySs make them valuable candidates for the utilization in power electronics converters
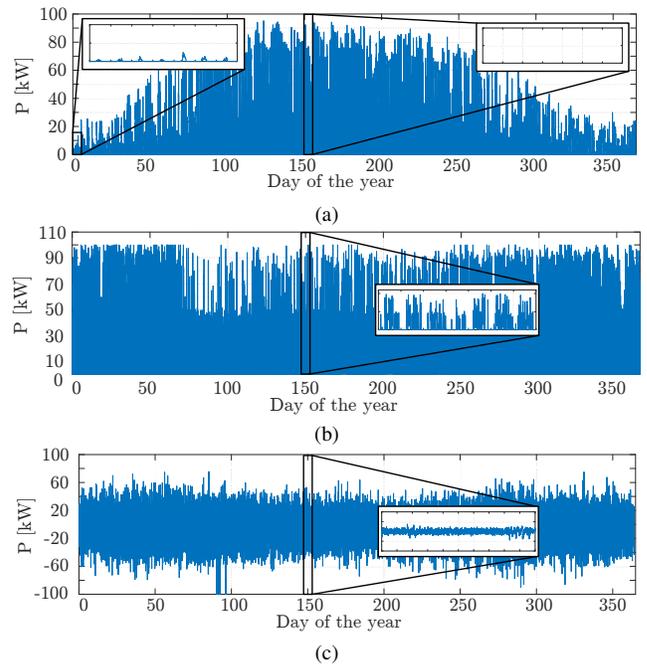

Fig. 22. Yearly mission profiles of a 100 kW 2L-VSC used as (a) PV central inverter, with zoom in two weeks of low and high solar irradiation, (b) as FCS grid connected converter, with zoom in one week, and (c) as grid interface for a BESS providing frequency regulation, with zoom in one day.

for multiple applications. As shown in the previous sections, both HySs concepts exhibits excellent switching performances and lower cost than pure SiC MOSFETs, furthermore, tHySs have also low conduction losses at low partial load, both in forward and reverse conduction, since only the SiC MOSFET will be conducting, since to the junction barrier voltage of the Si IGBT, during forward conduction, and of the Si diode, during reverse conduction, will force the current to flow only through the MOSFET channel, as detailed in Section III. Nonetheless, the SiC MOSFET exhibits the lowest conduction losses at low partial load. In this section, the performances of HySs are compared with the pure Si and SiC switches when implemented in 2L-VSC performing a specific load profile that reflects different applications of the converter. The minimum cost designs illustrated in Fig. 18 are considered for the following study, as reflect the goal of competitive business. The selected applications consist of a PV inverter, an EV FCS converter, and a BESS converter, all rated with the specifications previously used for the chip area analysis. These applications are deployed in the Netherlands.

1) PV central inverter: Photovoltaic energy is a mature and consolidated application of power electronics converters. In such systems, 2L-VSC are widely applied as central inverters [46], interfacing the strings' MPPTs with the AC grid. A solar inverter's load profile is inherently affected by the PV plant's location since the solar irradiation on the ground is strongly influenced by the geographical location.

2) EV Fast Charging Station: Fast charging of EVs is a rising application of power electronics converters. In this application, a high power 2L-VSC is a well-suited circuit topology for interfacing the AC grid with multiple isolated DC-DC battery chargers connected at the dc side. The profile
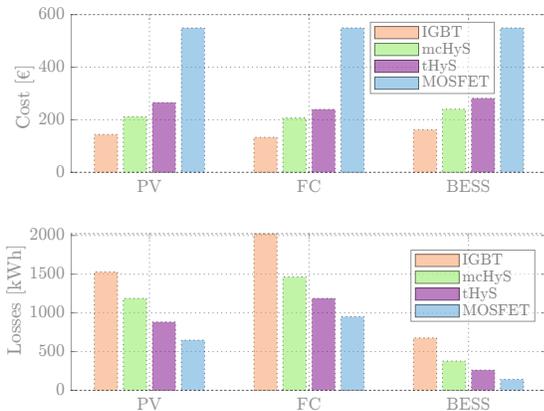
Fig. 23. Semiconductor cost and losses of 2L-VSCs assembled with various switch technologies performing the mission profiles shown in Fig. 22.

used for the study, provided by experts from a dutch DSO, consists of the aggregation of the measured profiles of two 50 kW chargers during one year.

3) BESS providing Primary Frequency Regulation: Primary frequency regulation (PFR) using grid-connected BESS is another growing area for power electronics converter [31], [47]. PFR consist of responding to the frequency variations of the grid with a droop logic, where the maximum power has to be delivered for deviations higher than ± 200 mHz, following the guidelines provided by the Dutch TSO [48]. A typical load profile of a BESS providing PFR would mostly consist of operation at very low partial loads, where HySs perform very well, due to the high inertia and regulating power of the central European transmission grid that effectively limit the frequency variations [49].

4) Switch comparison: The yearly mission profiles described are shown in Fig. 22. As it is possible to see the EV charging station has the profile that leads to the highest power utilization, followed by the PV, and the PFR application. On the other hand, the latter has a very high utilization rate, having the BESS working 98% of the considered time. The comparison of the switches for various applications is presented in Fig. 23, where cost and losses of an mcHyS-based 2L-VSC performing different mission profiles compared with an tHyS-based 2L-VSC. From the figure it can be noticed that the mcHyS provides a cheaper solution than the typical HyS, however it also shows slightly worse performances. Overall HyS provides a substantial cost saving with respect to SiC MOSFETs. On the performance side, the smaller SiC MOSFET of the mcHyS leads to slightly higher losses than the tHyS. Nonetheless, the improvement with respect to the IGBT solution is substantial, almost halving the losses over the yearly profile.

5) Limitation of the mcHyS: To summarize, the analysis presented in this section suggests that HySs are a valid cost-performance trade-off alternative to the common Si IGBT and SiC MOSFETs when applied in industrial power electronics applications. HySs can offer various degrees of loss saving and power density increase versus single technology

IGBT-based 2L-VSC. However, HySs, due to the fact that they are assembled through the paralleling of two active devices, presents also some drawbacks with respect to single technology switches. The main drawback consists in the fact that HyS requires two independent gate driving circuit per single switch, adding an extra cost versus single technology switches. However, in high power application, the costs of the extra gate driver is generally much lower than the power modules. An additional factor to consider for the mcHyS implementation is the commutation inductance between its elements. As shown in Section IV, a large inductance between the HyS components can be detrimental to its performances. In this context, it is of fundamental importance to consider a minimum distance between IGBTs and MOSFETs in PCB layout when discrete devices are used for the mcHyS realization. This issue could be solved packaging the Si-IGBT and SiC-MOSFET together in a custom power module, however, to the knowledge of the authors, such module is not a commercial product yet.

VII. CONCLUSION

In this paper, the conduction and switching performances of the mcHyS are experimentally characterized and compared with the one of SiC MOSFETs, Si IGBTs, and the tHyS concept. The experimental results proved that the analytical equations given for modeling HySs provided excellent accuracy and showed how HySs position themselves between the pure Si IGBTs and SiC MOSFETs in terms of performances and costs. Additionally, a 10kW 2L-VSC prototype has been assembled to test and benchmarked the efficiency of a mcHyS-based VSC versus single technology VSC. Furthermore, it was shown that the two additional switching events of the mcHyS happen in soft switching as long as the commutation inductance is minimized. Afterward, the switches have been compared in terms of chip area and thus in costs, upholding that the mcHyS provides a cheaper alternative to SiC MOSFETs and the commonly studied in literature tHyS. HyS have also been shown valuable candidates for 2L-VSC switches applied in three power electronics industrial applications: photovoltaic inverter, electric vehicle fast-charging station, and battery storage systems for grid ancillary service.

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