Comparison of Two and Three-Level DC-AC Converters for a 100 kW Battery Energy Storage System

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***Abstract*—This paper discusses a qualitative comparison between Two and Three-Level DC-AC converter topologies for battery energy storage applications. Three-Level Neutral Point Clamped (NPC) and T-Type circuit topologies are benchmarked versus the state-of-art Two-Level Voltage Source Converter in terms of efficiency and power density considering a 100 kW system. Analytical equations for determining the power losses in the semiconductors modules are given, and the procedure for designing the output *LCL* filter and the DC-link capacitors is described. The analysis, based on off-shelf circuit components, shows that Three-Level topologies perform better than the Two-Level one in both considered metrics, mainly due to their lower switching losses that allow operating at higher switching frequency without significantly degrading the system efficiency, and, at the same time, increasing the system power density. Additionally, it is found that the T-Type topology shows better performances than the NPC topology at high partial loads, being then more suitable for applications that require most of the operation at maximum power.**

I. Introduction

Battery energy storage systems are commonly interfaced with the distribution network through Power Electronics based DC-AC Voltage Source Converters (VSCs). The conventional Two or Three-Level circuits, depicted in Fig. 1, for Low to Medium voltage power conversion are mature technologies, and they have been widely applied for industrial electronics applications and renewable energy. For storage and solar applications, conventional three-phase Two-Level VSC, assembled with three half-bridge power modules, is the dominant circuit topology adopted by commercial products, mainly due to their robustness, low cost, and low complexity [1], [2]. Nonetheless, in other fields, such as motor drives and wind power, multilevel topologies found more market attention, especially for Medium-Voltage power conversion [3], [4].

Previous studies have shown how Three-Level topologies can outmatch the conventional Two-Level topology for high enough switching frequencies in terms of efficiency [5], [6]. In this paper such comparison is performed for DC-AC converters to be deployed for battery storage applications. The design of DC-AC converters for storage applications is subject to different design constraints and peculiarities from other power electronics applications, and so their design procedure can not be systematized based on the ones for other PE applications. Storage systems, in fact, require highly efficient bi-directional operation and, depending on the grid service provided by the system, significant reactive power generation capabilities. Additionally, storage systems are subject to the regulation of grid-connected systems, e.g., current harmonic injections, Low Voltage Ride Through, and voltage regulation at the point of common coupling [7], [8]. Another particularity of storage systems is related to the electrochemical battery, its impedance, in fact, strongly varies with the frequency, and its open-circuit voltage is related to the State of Charge (SoC) [9], affecting the converter's DC-link design.

In this paper, 100kW Three-Level T-Type and Neutral Point Clamped (NPC) topologies for battery storage systems are benchmarked in terms of efficiency and power density versus the Two-Level circuit topology. A low voltage DC-link is taken into consideration, compatible with the commercially available 89 kWh battery rack M3-R089 from Samsung [10]. The analytical equations for estimating the semiconductor losses and the procedure for designing the output *LCL* filter and the DC-link capacitors are described. The comparison shows that Three-Level converters can lead to higher efficiency and power density. Furthermore, it is seen that T-Type topologies lead to the overall highest efficiency at high partial loads, while the NPC circuit topology is more suitable for applications that require operating mostly at lower partial loads.

II. Three-Level Topologies

The single phase bridge of the circuit topologies considered in this study are displayed in Fig. 1. The Two-Level Converter (2LC), Fig. 1 (a), is the topology that requires the least semiconductors; thus, it has reduced complexity and costs. Moreover, this topology has low conduction losses, since only one component at the time conducts the impressed AC current, and, at low switching frequencies, it offers overall outstanding performances. Nonetheless, the NPC topology, Fig. 1 (b), for the same DC-link voltage, requires lower voltage rating of the IGBT modules, since the components have to block half the DC-link voltage, and thus it shows lower switching losses. Additionally, all components are of the same voltage class. The T-Type topology, Fig. 1 (c), instead, is assembled with components of two different voltage class, since the outer IGBTs, T_1 and T_4 have to block the full DC-link voltage; and then it is subject to higher switching losses than the NPC

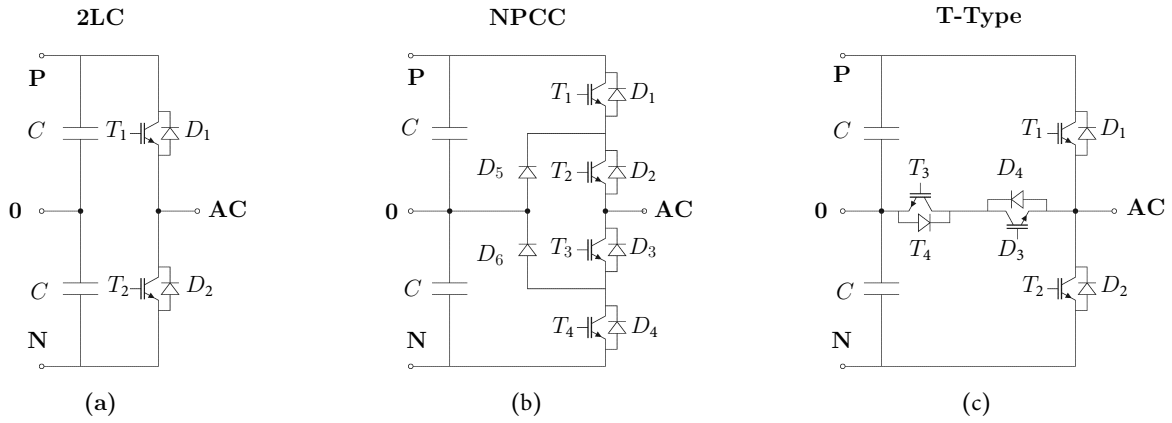

Fig. 1: Circuit topologies considered in this study: single phase-bridge of (a) Two-Level, (b) Three-Level Neutral Point Clamped, and (c) Three-Level T-Type voltage source converters.

due to the intrinsically lower switching performances of the higher voltage class devices. However, the terminal AC current conduction occurs through one semiconductor, when it is not flowing through mid-point of the DC-link.

For this study, the battery rack M3-R089 from Samsung has been considered [10]. Then, for 2LC and 3LC-TTYPE topologies, IGBT modules with 1200V voltage class are selected. The 3LC-NPC, instead, allows the selection of a lower voltage rating, so the 600V voltage class is chosen. The converter AC output voltage is fixed to 400V line to line, and so the commercially available SKM300GB12T4, SEMiX305MLI07E4, SEMiX305TMLI12E4B TrenchGate IGBT4 modules rated 300A are considered [11].

III. Semiconductor Efficiency

The power losses in the semiconductors can be analytically calculated based on the assumption that the switching frequency f_s is much greater than the grid frequency f_g. According to such assumption and considering sinusoidal Pulse-Width-Modulation (PWM), the sinusoidal carrier can be considered constant during one switching period. Then, given the on-state characteristics of IGBTs and diode, modelled as a V_i and r_i circuit, the conduction losses are analytically predicted as function of the RMS and average current flowing through the component as:

$$P_\mathrm{c} = V_\mathrm{i} \cdot I_\mathrm{avg,i} + r_\mathrm{i} \cdot I^2_\mathrm{rms,i} \tag{1}$$

The switching losses, instead, are function of the switching energies $E_\mathrm{on,off,rr}$ and they have to be scaled according to the switched voltage V_dc and the data-sheet reference voltage V_b:

$$P_\mathrm{s} = \frac{f_\mathrm{s} V_\mathrm{dc}}{4\pi V_\mathrm{b}} \int E_\mathrm{on,off,rr} \mathrm{d}t. \tag{2}$$

Furthermore, the switching energies, and as well as the on-state parameters, are temperature dependant and they can be linearized as function of the junction temperature. Then, to evaluate the losses, it is necessary to find the expression of the average and RMS current through the semiconductor. In the following the current expressions are given, where the phase shift of the current with respect to the voltage at the fundamental frequency is indicated with δ, m indicates the modulation index, and $\hat{I}_\mathrm{ac}$ is the peak output AC current. The components denomination is done according to Fig. 1.

A) Two-Level Converter:

$$I_{\mathrm{avg,T_{1,2}}} = m\frac{\hat{I}_\mathrm{ac}}{8\pi}(m\pi\cos\delta + 4) \tag{3}$$

$$I_{\mathrm{avg,D_{1,2}}} = m\frac{\hat{I}_\mathrm{ac}}{8\pi}(4 - m\pi\cos\delta) \tag{4}$$

$$I_{\mathrm{rms,T_{1,2}}} = \frac{\hat{I}_\mathrm{ac}}{2}\sqrt{\frac{8m\cos\delta + 3\pi}{6\pi}} \tag{5}$$

$$I_{\mathrm{rms,D_{1,2}}} = \frac{\hat{I}_\mathrm{ac}}{2}\sqrt{\frac{3\pi - 8m\cos\delta}{6\pi}} \tag{6}$$

B) Three-Level Neutral Point Clamped Converter:

$$I_{\mathrm{avg,T_{1,4}}} = m\frac{\hat{I}_\mathrm{ac}}{4\pi}\Big[(\pi - |\delta|)\cos|\delta| + \sin|\delta|\Big] \tag{7}$$

$$I_{\mathrm{avg,T_{2,3}}} = m\frac{\hat{I}_\mathrm{ac}}{4\pi}(m|\delta|\cos|\delta| - m\sin|\delta| + 4) \tag{8}$$

$$I_{\mathrm{avg,D_{1,2,3,4}}} = m\frac{\hat{I}_\mathrm{ac}}{4\pi}(\sin|\delta| - |\delta|\cos|\delta|) \tag{9}$$

$$I_{\mathrm{avg,D_{5,6}}} = \frac{\hat{I}_\mathrm{ac}}{2\pi}\left[m\left(|\delta| - \frac{\pi}{2}\right)\cos|\delta| - m\sin|\delta| + 2\right] \tag{10}$$

$$I_{\mathrm{rms,T_{1,4}}} = \hat{I}_\mathrm{ac}(1 + \cos\delta)\sqrt{\frac{m}{6\pi}} \tag{11}$$

$$I_{\mathrm{rms,T_{2,3}}} = \frac{1}{2}\sqrt{\frac{\hat{I}_\mathrm{ac}(2m\cos\delta(2 - \cos\delta) + 3\pi - 2m)}{3\pi}} \tag{12}$$

$$I_{\mathrm{rms,D_{1,2,3,4}}} = \hat{I}_\mathrm{ac}(1 - \cos\delta)\sqrt{\frac{m}{6\pi}} \tag{13}$$

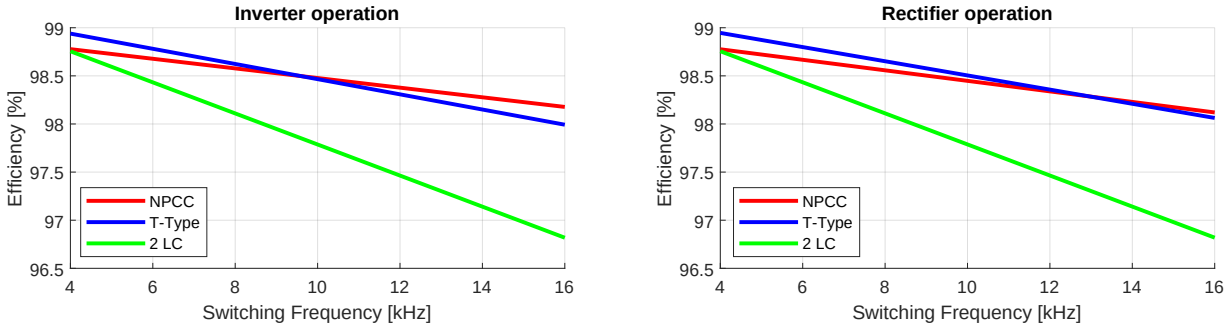

Fig. 2: Semiconductor efficiency of three-level and two-level topologies at maximum power for inverter (a) and rectifier (b) operation varying the switching frequency.

$$I_{\mathrm{rms,D_{5,6}}} = \frac{\hat{I}_{\mathrm{ac}}}{2}\sqrt{\frac{(+3\pi - 2m(\cos 2\delta + 3))}{3\pi}} \tag{14}$$

C) Three-Level T-Type Converter:

$$I_{\mathrm{avg,T_{1,4}}} = m\frac{\hat{I}_{\mathrm{ac}}}{4\pi}\left[(\pi - |\delta|)\cos|\delta| + \sin|\delta|\right] \tag{15}$$

$$I_{\mathrm{avg,T_{2,3},D_{2,3}}} = m\frac{\hat{I}_{\mathrm{ac}}}{2\pi}\left[m(|\delta| - \frac{\pi}{2})\cos|\delta| - m\sin|\delta| + 2\right] \tag{16}$$

$$I_{\mathrm{avg,D_{1,4}}} m\frac{\hat{I}_{\mathrm{ac}}}{4\pi}(\sin|\delta| - |\delta|\cos|\delta|) \tag{17}$$

$$I_{\mathrm{rms,T_{1,4}}} = \hat{I}_{\mathrm{ac}}(1 + \cos\delta)\sqrt{\frac{m}{6\pi}} \tag{18}$$

$$I_{\mathrm{rms,T_{2,3},D_{2,3}}} = \frac{\hat{I}_{\mathrm{ac}}}{2}\sqrt{\frac{3\pi - 4m(\cos^2\delta + 1)}{3\pi}} \tag{19}$$

$$I_{\mathrm{rms,D_{1,4}}} = \hat{I}_{\mathrm{ac}}(1 - \cos\delta)\sqrt{\frac{m}{6\pi}} \tag{20}$$

The switching losses are found integrating the switching energy as a function of the switched current during the switching time of each component. The switching energies are interpolated from the components data-sheet and expressed as second-order polynomial functions.

A) Two-Level Converter:

$$P_{\mathrm{s,T_{1,2},D_{1,2}}} = \frac{f_s U_{\mathrm{dc}}}{2\pi U_{\mathrm{B}}}\left[\frac{\pi b_2 \hat{I}_{\mathrm{ac}}^2}{2} + \pi b_0 + 2b_1\hat{I}_{\mathrm{ac}}\right] \tag{21}$$

B) Three-Level Neutral Point Clamped Converter: The switching losses are found through:

$$P_{\mathrm{s,T_{1,4},D_{5,6}}} = \frac{f_s U_{\mathrm{dc}}}{4\pi U_{\mathrm{B}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\delta - \pi + \sin\delta\cos\delta)}{2} + b_1\hat{I}_{\mathrm{ac}}(1 + \cos\delta) + b_0(\delta - \pi)\right] \tag{22}$$

$$P_{\mathrm{s,T_{2,3},D_{1,4}}} = \frac{f_s U_{\mathrm{dc}}}{4\pi U_{\mathrm{B}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\delta - \cos\delta\sin\delta)}{2} + b_1\hat{I}_{\mathrm{ac}}(1 - \cos\delta) + b_0\delta\right] \tag{23}$$

C) Three-Level T-Type Converter:

$$P_{\mathrm{s,T_{1,4},D_{2,3}}} = \frac{f_s U_{\mathrm{dc}}}{4\pi U_{\mathrm{B}}}\left[b_2\hat{I}_{\mathrm{ac}}^2\frac{(\pi - \delta + \sin\delta\cos\delta)}{2} + b_1\hat{I}_{\mathrm{ac}}(1 + \cos\delta) + b_0(\delta - \pi)\right] \tag{24}$$

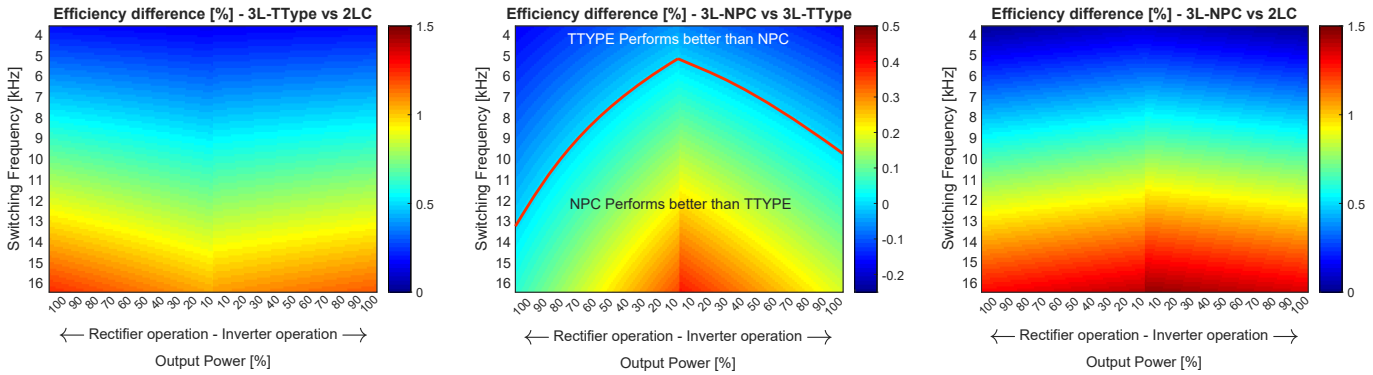

Fig. 3: Semiconductor efficiency gain between Three-Level and Two-Level topologies and between T-Type and NPC varying the output power and the switching frequency for a modulation index m=0.725.

$$P_{\mathrm{s,T_{2,3},D_{1,4}}} = \frac{f_s U_{\mathrm{dc}}}{4\pi U_{\mathrm{B}}}\left[b_2 \hat{I}_{\mathrm{ac}}^2 \frac{(\delta - \cos\delta \sin\delta)}{2} + b_1 \hat{I}_{\mathrm{ac}}(1-\cos\delta) + b_0\delta \right] \quad (25)$$

Fig. 2 displays the semiconductor efficiency of Two and Three-Level topologies at maximum power for inverter and rectifier operation varying the switching frequency, for a junction temperature of 150°C. What stands out is the declining of the Two-Level efficiency for high switching frequencies. The Three-Level topologies, in fact, show better performances for higher switching frequencies due to the lower switching energies. Additionally, in Fig. 3, the efficiency gain between the Three-Level circuit topologies versus the Two-Level and between the Neutral-Point Clamped and the T-type are displayed, varying both the switching frequency and the output power. As expected, the highest efficiency gain is for high switching frequencies. However, it can be noted that the NPC offers better performances at low partial loads, while the T-Type shows the opposite behaviour. Such consideration can be useful when designing the battery storage DC-AC converter for a specific application, e.g., for a mission profile that foresee high operation at low partial load, the T-Type topology can offer more considerable advantages at higher powers and moderate switching frequencies, i.e., <12 kHz.

IV. LCL Filter Design

Battery storage systems are connected to the electrical network; thus, they need to respect the connection rules imposed by the standards, e.g., the EN 50160 [8], regulating the voltage of distribution systems, and IEEE 519-2014 [7], regulating the current harmonics injection in the network. PWM operated VSCs inherently generate voltage harmonics in the AC terminal, and in this context, a *LCL* filter is adopted to attenuate the resulting current harmonics injected in the grid to be compliant to the standards. The voltage harmonic spectrum produced by PWM modulated Two-Level and Three-Level converter can be calculated through the Bessel function as described in [12]. Three-Level topologies have a lower harmonic content in the AC output in respect to Two-Level topologies [12], [13]. Then, they require a lower attenuation by the filter and so a lower total inductance value L_{tot} [14].

The design of the output *LCL* filter has to guarantee the attenuation of the high order harmonics, e.g., according to the standard IEEE 519-2014 I_{h} with h>35 has to be lower than 3% the nominal 50Hz current. The harmonic attenuation given by *LCL* filters can be approximated by [15]:

$$Att \approx \frac{1}{L_{\mathrm{c}} L_{\mathrm{g}} C \omega_{\mathrm{h}}^3} \quad (26)$$

where L_{c} L_{g} C are respectively the converter side and grid side inductance and the capacitor and $\omega_h = 2\pi f_{\mathrm{h}}$ represents the first group of harmonics to be attenuated, generally a low order side-band of the switching frequency. The resonance frequency of the filter f_{res} is generally chosen between $\frac{1}{6} f_{\mathrm{s}}$ and $\frac{1}{2} f_{\mathrm{s}}$, when the converter is controlled through the grid side current [16], in order that the digitally controlled VSC with sampling acquisition of $T_{\mathrm{s}} = {}^1/_{f_{\mathrm{s}}}$ falls into the stable region, and it is defined by the filter components as:

$$\omega_{\mathrm{res}} = 2\pi f_{\mathrm{res}} = \sqrt{\frac{L_{\mathrm{c}} + L_{\mathrm{g}}}{L_{\mathrm{c}} L_{\mathrm{g}} C}}. \quad (27)$$

From Equation (26) it can be noted that increasing ω_{h} the filter delivers the same attenuation with lower values of inductances and/or capacitance. Then, concerning the *LCL* output filter, the advantage of Three-Level topologies over Two-Level topologies is two-fold. First, a lower attenuation by the filter is required and so a lower total inductance. Secondly, the Three-Level topologies are well suitable for high switching frequencies, due to their excellent efficiency, and so the higher switching frequency leads to a reduced size of the output *LCL* filter.

Following the procedure illustrated in [17], several possible filter designs are evaluated in terms of weight, volume and losses at full power. The winding losses of litz (Cu) wires are analytically calculated based on the method proposed in [18], while the core losses of toroidal power cores are calculated through the improved Generalized Steinmetz Equation *iGSE* [19]. Several core materials from [20] are considered, and the designs are checked for a maximum inductor temperature of 150°C. The power losses in the *LCL* capacitors are calculated according to the leakage current and the dissipation factors, derived from manufacturers data-sheet [21], [22]. The *LCL* filter is then designed for several switching frequencies, and the Pareto fronts are displayed in Fig. 4, where the symbols differentiate between Two and Three-Level topologies and the colours between switching frequencies. As expected, it stands out that increasing the switching frequency higher power density and efficiency can be achieved. Besides, under the same switching frequency, Three-Level topologies offer better *LCL* filter power density and efficiency.

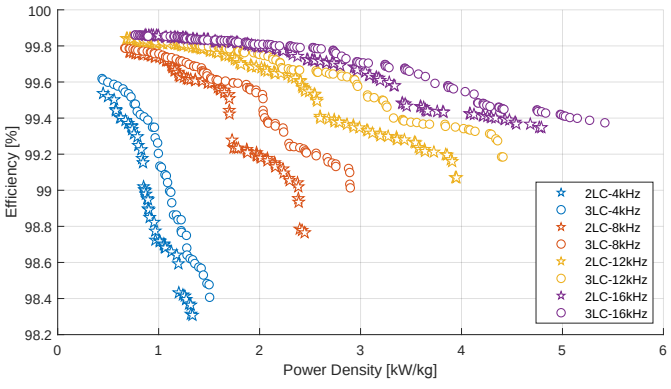

Fig. 4: Efficiency and power density of output *LCL* filter designs for two and three level converters and for several switching frequencies.

V. DC-Link Design

Typically the DC-link capacitors in voltage source converters act as an energy buffer between the input and output of the converter [23]. In fact, for the three wire converters depicted in Fig. 1, without considering over modulation, the peak AC phase voltage has to be always below half the DC-link voltage:

$$\frac{V_{\mathrm{dc,min}}}{2} - \frac{\Delta V_{\mathrm{dc,r}}}{2} \geq \hat{V}_{\mathrm{ac,max}} \tag{28}$$

Then, considering the minimum battery DC voltage, and a $+/-10\%$ variation of the AC voltage from the nominal value, the maximum allowed voltage ripple is 55V. In this respect, the DC voltage ripple in Two-Level converters in case of balanced operation is driven by the high frequency components of the DC-link current and it can be predicted as [24]:

$$\Delta V_{\mathrm{dc,2LC}} = \frac{3M\hat{I}_{\mathrm{ac}}\cos\varphi}{8f_{\mathrm{s}}C_{\mathrm{dc}}}(1+M) \tag{29}$$

where C_{dc} is the DC-link capacitance value. In Three-Level converters, modulated with sinusoidal PWM, the DC-link current shows a third harmonic component. Such low frequency harmonic dominates the higher frequencies ones and drives the DC-link voltage ripple:

$$\Delta V_{\mathrm{dc,3LC}} = \frac{I_3}{3C\pi f_{\mathrm{g}}} \tag{30}$$

where the third harmonic current I_3 can be calculated as [25]:

$$I_3 = \frac{6MI_{\mathrm{pk}}}{5\pi}\left(\frac{2\cos\varphi}{3} + j\sin\varphi\right). \tag{31}$$

If the third harmonics is mitigated through space vector modulation, the DC voltage ripple is driven by the effect of the high-frequency components, as for the Two-Level, and then it is reduced. Techniques for suppressing the low-frequency oscillation in the DC capacitors of Three-Level converters have been proposed in literature [13], [26]. However, the applicability of such techniques is limited or by the power factor and/or by the modulation index [13], or by the necessity of installing additional circuitry [26]. For the case of battery storage systems implementing single stage power conversion as depicted in Fig. 1, there is no control over the modulation index, since both the DC side and AC side voltages are fixed respectively by the battery and the AC network unless a two-stage system is considered. Moreover, it is often required the four-quadrant operation; thus, the region where the third harmonic can be cancelled is limited [13]. In this context, the DC link is generally designed to mitigate the voltage ripple produced by the third harmonic.

Concerning the energy requirements, the DC capacitors are also designed in order to be able to sustain a load step ΔP in a time period T_{r}, allowing a maximum voltage deviation of ΔV_{dc} [27]. Then the minimum capacitance value is given by:

$$C_{\mathrm{dc,e}} \geq \frac{T_{\mathrm{r}} \cdot \Delta P}{(2 \cdot V_{\mathrm{dc}}\Delta V_{\mathrm{dc}})} \tag{32}$$

where T_{r} depends on the converter control delay and it is usually selected as 5 to 10 modulation periods [27]. Both Two and Three-Level topologies are subject to this requirement.

TABLE I: Capacitance values to guarantee the required energy buffer and limit the voltage ripple

Ripple		Energy
2LC 0.29 mF	3LC 2.93 mF	2LC / 3LC 0.49 mF

According to the design specifications, the capacitance values that guarantee an adequate energy buffer and limits the voltage ripple are listed in Table I. As it is possible to see, the Three-Level topology requires a much higher capacitance to limit the voltage ripple, due to the presence of the third harmonic current. Furthermore, the electrolytic capacitors have to withstand the ripple current. The DC capacitor RMS current is the same for both Two and Three-Level converters [28], and it is analytically calculated through [29]:

$$I_{\mathrm{dc-cap}} = \hat{I}_{\mathrm{ac}}\sqrt{M\left[\frac{\sqrt{3}}{4\pi} + \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\cos^2\phi\right]}. \tag{33}$$

Electrolytic capacitors do not have high current capabilities, and then, their design usually leads to over dimensioning the DC-link capacitance value in order to satisfy the current capability limitations, mainly defined by the desired minimal life-time of these components. For this reason, the DC-link design, in terms of components selections, does not present significant differences between Two and Three-Level converters. For example, considering the commercial capacitors of the $500V_{\mathrm{dc}}$ class from [21], the DC-link is designed considering parallel strings of two series capacitors. The number of parallel strings is function of the maximum $I_{\mathrm{dc-cap}}$. The obtained designs are checked in terms of minimum capacitance, to satisfy the requirements of Table I, and minimum life-time of 20 years using the lifetime model given in [22]. The feasible solutions are plotted in Fig. 5 and it can be seen that the design with the lowest capacitance is found around 4 mF, more than the minimum required capacitance shown in Table I.

VI. Conclusions and Future Work

In this paper the design of semiconductors, *LCL* filter, and DC-link capacitors for battery energy storage converters

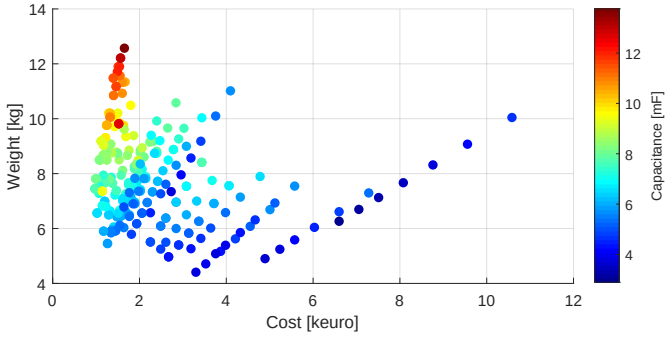

Fig. 5: Weight, costs and capacitance of the feasible DC-link capacitors designs selecting components from [21].

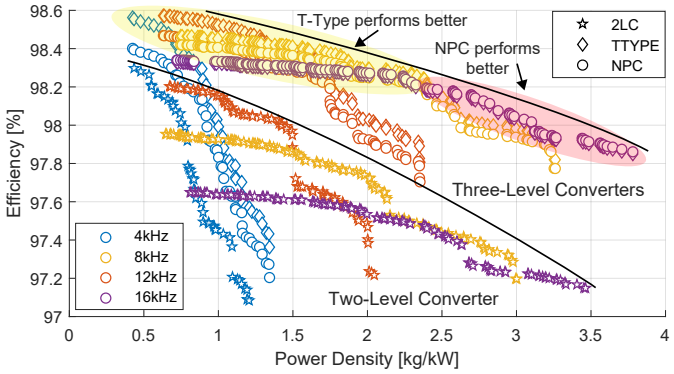

Fig. 6: System power density and efficiency at full power in inverter operation for different topologies and f_s.

considering Two and Three-Level circuit topologies have been discussed. It has been shown that Three-Level topologies have lower semiconductor losses and that their efficiency does not decrease as much as the Two-Level one for high switching frequencies. It has also been shown that the T-type topology outperforms the NPC for moderate switching frequencies, i.e., $f_s \leq$12 kHz, and high partial loads. In this context, the T-type might be favourite for applications that require long operation at full power, while the NPC when operating mostly at low partial loads. Additionally, several feasible designs for the *LCL* filters and the DC-link capacitors have been shown. From Fig. 4 it is clear that increasing the switching frequency, lighter and more efficient filters can be designed. Regarding the DC-link, the procedure for its design has been illustrated, and it was shown how the poor current capability of aluminium electrolytic capacitors influences the design and leads to over dimensioning of the DC-link in terms of capacitance value. The full system power density and efficiency at full power, considering a DC link design with a weight of 7kg, are displayed in Fig. 6. It can be seen that three-level converters perform significantly better both in terms of power density and efficiency since they do not suffer too much with the increase of switching frequency, thus resulting in higher power densities. Additionally, it is seen how T-Type topologies lead to the overall highest efficiency, while the NPC at higher switching frequencies represents a good trade-off between power density and efficiency.

Future work will be focused on the experimental validation of the semiconductor and *LCL* filter models here described. Further analysis will be focused on relating the converter design with the battery storage application, introducing mission profiles in the study.

References

[1] S. Vazquez, S. M. Lukic, E. Galvan, L. G. Franquelo, and J. M. Carrasco, "Energy storage systems for transport and grid applications," *IEEE Trans. Ind. Electron.*, 2010.

[2] K. Samir, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-Connected Photovoltaic Systems," *IEEE Ind. Electron. Mag.*, 2015.

[3] T. B. Soeiro, S. Member, and J. W. Kolar, "The New High-Efficiency Hybrid Neutral-Point-Clamped Converter," *IEEE Trans. Ind. Electron.*, 2013.

[4] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, 2013.

[5] T. B. Soeiro, M. Schweizer, J. Linner, P. Ranstad, and J. W. Kolar, "Comparison of 2- and 3-level Active Filters with Enhanced Bridge-Leg Loss Distribution," in *8th Int. Conf. Power Electron. - ECCE Asia*, 2011.

[6] M. Schweizer, S. Member, and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," *IEEE Trans. Power Electron.*, 2013.

[7] IEEE Standards Association, "IEEE Std. 519-2014. IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," 2014.

[8] CENELEC, "EN 50160 - Voltage characteristics of electricity supplied by public distribution systems," *Eur. Stand.*, 2010.

[9] C. Brivio, V. Musolino, M. Merlo, and C. Ballif, "A Physically-Based Electrical Model for Lithium-Ion Cells," *IEEE Trans. Energy Convers.*, 2019.

[10] Samsung SDI, "ESS Batteries by Samsung SDI," 2019. [Online]. Available: https://www.samsungsdi.com/ess/index.html

[11] "Semikron." [Online]. Available: https://www.semikron.com/products/product-classes/igbt-modules.html

[12] D. G. Holmes and T. A. Lipo, "Modulation of ThreePhase Voltage Source Inverters," *Pulse Width Modul. Power Convert.*, 2010.

[13] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, 2000.

[14] K. Jalili and S. Bernet, "Design of LCL filters of active-front-end two-level voltage-source converters," *IEEE Trans. Ind. Electron.*, 2009.

[15] K. B. Park, R. M. Burkart, B. Agostini, and T. B. Soeiro, "Application of 1.7-kV 700-A SiC LinPak to Optimize LCL Grid-Tied Converters," *ICPE 2019 - ECCE Asia - 10th Int. Conf. Power Electron. - ECCE Asia*, 2019.

[16] Y. Wu, A. Shekhar, T. B. Soeiro, and P. Bauer, "Voltage Source Converter Control under Distorted Grid Voltage for Hybrid AC-DC Distribution Links," *IECON 2019 - 45th Annu. Conf. IEEE Ind. Electron. Soc.*, 2019.

[17] K. B. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, "Weight Minimization of LCL Filters for High-Power Converters: Impact of PWM Method on Power Loss and Power Density," *IEEE Trans. Ind. Appl.*, 2017.

[18] J. A. Ferreira, "Improved Analytical Modeling of Conductive Losses in Magnetic Components," *IEEE Trans. Power Electron.*, 1994.

[19] J. Reinert, A. Brockmeyer, and R. W. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Trans. Ind. Appl.*, 2001.

[20] Chang Sung. [Online]. Available: http://www.changsung.com/

[21] Cornell Dubilier, "500C Capacitors." [Online]. Available: https://www.cde.com/capacitors/aluminum-electrolytic/screw-terminal

[22] Cornell Dublier, "Aluminum Electrolytic Capacitor Application Guide," Tech. Rep.

[23] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Trans. Ind. Appl.*, 2014.

[24] X. Pei, W. Zhou, and Y. Kang, "Analysis and Calculation of DC-Link Current and Voltage Ripples for Three-Phase Inverter With Unbalanced Load," *IEEE Trans. Power Electron.*, 2015.

[25] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Analysis of dc-link capacitor current in three-level neutral point clamped and cascaded H-bridge inverters," *IET Power Electron.*, 2013.

[26] J. Moia and M. L. Heldwein, "Carrier-based modulation technique to reduce low frequency ripple at the partial DC-link voltages of a three-level/-phase/-wire NPC converter applied to future DC bipolar active distribution networks," *PCIM Eur. 2016; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag.*, 2016.

[27] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, "Ac/dc/ac PWM converter with minimum energy storage in the DC link," *Conf. Procedings - IEEE Appl. Power Electron. Conf. Expo. - APEC*, 1993.

[28] G. I. Orfanoudakis, S. M. Sharkh, and M. A. Yuratich, "Analysis of DC-link capacitor losses in three-level Neutral Point Clamped and Cascaded H-Bridge voltage source inverters," *IEEE Int. Symp. Ind. Electron.*, 2010.

[29] J. W. Kolar and S. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *IEE Proceedings-Electric Power Appl.*, 2005.