Stability and Accuracy Analysis of a Distributed Digital Real-Time Co-simulation Infrastructure

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***Abstract*—Co-simulation techniques are gaining popularity amongst the power system research community to analyse future scalable Smart Grid solutions. However, complications such as multiple communication protocols, uncertainty in latencies are holding up the widespread usage of these techniques for power system analysis. These issues are even further exacerbated when applied to Digital Real-Time Simulators (DRTS) with strict real-time constraints for Power Hardware-In-the-Loop (PHIL) tests. In this paper, we present an innovative Digital Real-Time Co-simulation Infrastructure that allows interconnecting different DRTS through the Aurora 8B/10B protocol to reduce the effects of communication latency and respect real-time constraints. The proposed solution synchronizes the DRTS interconnection by means of the IEEE 1588 Precision Time Protocol (PTP) standard to align executions and results obtained by the co-simulated scenario. The Ideal Transformer Method (ITM) Interface Algorithm (IA), commonly used in PHIL applications, is used to interface the DRTS. Finally, we present time-domain and frequency-domain accuracy analyses on the obtained experimental results to demonstrate the potential of the proposed infrastructure. With the presented setup, a time step duration down to $50\,\mu$s is shown to be stable and accurate in running an Electro-Magnetic Transients (EMT) co-simulated power grid scenario by interconnecting two commercial DRTS (i.e. RTDS NovaCor), extending the scalability of future Smart Grid real-time simulations.**

***Index Terms*—Power System Analysis, Smart Grid, Digital Real-time Simulators, Co-simulation Techniques, Numerical Stability.**

ACRONYMS

DSO	Distribution System Operator
DSP	Digital Signal Processor
DRTS	Digital Real-Time Simulator
DUT	Device Under Test
EMTP	Electro-Magnetic Transients Program
E2E	End-to-End
EMT	Electro-Magnetic Transients
FMI	Functional Mock-up Interface
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
HIL	Hardware-In-the-Loop
I/O	Input/Output
ICT	Information and Communication Technologies
IED	Intelligent Electronic Device
ITM	Ideal Transformer Method
IA	Interface Algorithm
PSD	Power Spectral Density
P2P	Peer-to-Peer
PTP	Precision Time Protocol
PSUT	Power System Under Test
PHIL	Power Hardware-In-the-Loop
RMS	Root Mean Square
RISC	Reduced Instruction Set Computer
ROS	Rest Of the System
SFP	Small-form Factor Pluggable
TSO	Transmission System Operator
TC	Transparent Clock
TCP	Transmission Control Protocol
UDP	User Datagram Protocol

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I. INTRODUCTION

In the last few years, robust research effort has been undertaken in computer-aided power system analysis for designing, developing, and testing future Smart Grids. Different domain-specific software simulation tools have been developed to emulate innovative functionalities and/or specific components of innovative power networks with high precision and accuracy [1]. In particular, time-domain modelling is crucial in the planning, design, and operation of modern power transmission systems.

Owing to the limits of pure software-based simulations, rising interest in testing real-world hardware has focused power system researchers' attention on real-time simulation [2]. Such a paradigm refers to a software model of a physical system that can execute at the same rate as the real-world physical system following the *wall clock* time. Simulations of such a paradigm are performed in a discrete constant time-stepped environment (i.e. fixed time step simulation) in which they must solve the internal state equation of the system under test in less time than the fixed time step duration. Conversely, an over-run error occurs. The time constraint of a real-time simulation varies depending on the application: transient stability studies, for example, can be performed with phasors based simulations with a time step duration in the range of 10 ms. On the other hand, Electro-Magnetic Transients (EMT) simulations require around tens of microseconds fixed time step duration to depict the detailed dynamics of large AC systems [3].

To this purpose, innovative multiprocessor architecture (e.g. IBM® Power8) and Field Programmable Gate Array (FPGA) have been proposed as a suitable solution to ensure hardware acceleration of EMT analysis [4] to respect real-time constraints. Moreover, such technologies ensure fast Digital and Analogue Input/Output (I/O) facilities to create the closed-loop interface with a real power system component, allowing Power Hardware-In-the-Loop (PHIL) to test its functionalities in a protected environment (i.e. laboratory setup). PHIL avoids huge costs in deploying such a component in the real world and shortens the design cycle. Nevertheless, PHIL is subject to stability and accuracy issues due to the latency of communication and power amplifier harmonic distortions between the power Device Under Test (DUT) and the simulated Rest Of the System (ROS). For this reason, different Interface Algorithms (IA) have been proposed in the literature to mitigate the effect of communication latency and stabilise the overall system under test [5], such as the Ideal Transformer Method (ITM).

The main difficulty for commercial Digital Real-Time Simulator (DRTS) is the significant computational resources required for the solution of detailed EMT models, thereby limiting the size of the AC system that can be accurately simulated [6]. In fact, a growing effort of the power system research community is concentrating on combining two or more DRTS, exploiting novel methodologies, communication protocols, and standards [7], such as co-simulation techniques [8]. Co-simulation techniques belong to Information and Communication Technologies (ICT) where a global simulation of a complex system can be achieved by composing the simulations of all its parts. Each simulator of a co-simulation presents itself to the other simulators as a black-box that exhibits the behaviour, consuming inputs, and producing outputs. Co-simulation techniques can be compared by using different definitions, as follows:

i) Homogeneous vs. heterogeneous co-simulation: In homogeneous co-simulation, different instances of a simulator are joined in a co-simulation framework to deal with the need of extending and scaling up the simulated scenario. Vice versa, heterogeneous co-simulation aims at joining different standalone simulators that focus their attention on a precise perspective of a complex system;

ii) On-site vs. multi-site co-simulation: This definition deals with the ICT interconnection and the geographical proximity of simulators composing the co-simulation framework. On-site co-simulation exploits fast communication protocols (e.g. Aurora 8B/10B) to ensure the local distribution of simulators and to enable analysis requiring low time step duration (e.g. EMT analysis in power systems). Multi-site co-simulation instead exploits Internet protocols (e.g. Transmission Control Protocol (TCP) or User Datagram Protocol (UDP)) to interconnect geographically distributed simulators in different laboratories far away from each other;

iii) Real-time vs. non-real-time co-simulation: In a Real-time co-simulation, all the involved simulators must implement a strict time synchronisation and time regulation schema and fast communication protocol to exchange data. This ensures that all real-time simulators could run their simulation without incurring in overruns and without deteriorating the numerical stability w.r.t. a standalone simulation. These co-simulation infrastructures could allow Hardware-In-the-Loop (HIL) and Power Hardware-In-the-Loop (PHIL) applications without damaging the interconnected hardware. Instead, a non-real-time co-simulation cannot perform HIL or PHIL tests because simulators cannot deal with real hardware; however, they can run the co-simulation faster than the wall-clock time, thus, enhancing the time span of a simulation scenario.

These definitions are not mutually exclusive. Indeed, a hybrid co-simulation framework can implement features of the previous definitions in a single solution.

In power system research, such techniques allow splitting the power system under analysis into sub-networks, each one executed on a DRTS, exploiting high-bandwidth communication channels (e.g. IEEE 802.3) to exchange interface voltages and currents between each other. However, such interconnections could lead to numerical instability and accuracy issues due to communication latency among DRTS like in the case of PHIL.

In this paper, we present a Distributed Digital Real-Time Co-simulation Infrastructure that allows the point-to-point interconnection of two DRTS (e.g. RTDS Technologies NovaCor). This architecture is a homogeneous, on-site, and real-time hybrid co-simulation framework that aims at extending the scalability of the Power System Under Test (PSUT) by splitting it on different DRTS that exchange data through communication protocols. Moreover, the infrastructure reach a numerical stability of the solution comparable to a standalone simulation that enable PHIL testing. The communication protocol used is Aurora 8B/10B and the time synchronisation schema of the co-simulation infrastructure is achieved by IEEE1588 Precision Time Protocol (PTP) [9]. The key contributions of this paper are as follows: *i)* innovating the DRTS co-simulation paradigm by exploiting Aurora 8B/10B to reduce the communication latency between two DRTS fulfilling a homogeneous co-simulation and extending the scalability of a simulated PSUT by exploiting the Ideal Transformer Method (ITM) Interface Algorithm (IA) for splitting it across the two DRTS; *ii)* permitting on-site co-simulations among DRTS to allows pure power system EMT without deteriorating the numerical stability of the PSUT solution; *iii)* exploiting a complex time synchronisation and regulation schema leveraging upon IEEE1588 PTP to align internal clock of each DRTS, to ensure a real-time co-simulation and to enable PHIL tests.

Moreover, this paper extends our previous work [10] with the following contribution: *i)* the proposed infrastructure is tested over a real interconnection of two DRTS racks exploiting the Digital Real-Time Co-simulation Infrastructure; *ii)* the infrastructure applies IEEE1588 PTP time synchronisation schema that aligns the internal clocks of both DRTS racks to the Global Positioning System (GPS) reference clock; *iii)* the results coming from the two different DRTS are compared and aligned by exploiting the IEEE1588 PTP time synchronisation schema; *iv)* time- and frequency-domain accuracy results are obtained for two different scenarios, namely the *worst-case* scenario that represents the latency limit that impacts the ITM IA stability with a time step duration of $500\,\mu s$ and the *average case* scenario in which the same circuit is run with a standard

time step duration for EMT analysis (i.e. $50\,\mu s$).

The structure of this paper is as follows. Section II provides a review on DRTS architecture. Then, a literature review on frequency-domain stability and time-domain accuracy analysis of PHIL IA that inspired our theoretical analysis on DRTS interconnection will follow. Section III introduces the co-simulation concepts and provides a comprehensive description of the co-simulation challenges still open. Section IV presents the proposed distributed Digital Real-Time Co-simulation Infrastructure and the laboratory setup implemented to test its functionalities. This section also describes the application of PHIL ITM IA to the proposed infrastructure and undertakes its frequency-domain stability analysis. Section V presents the experimental results to assess the time-domain and frequency-domain accuracy of the proposed solution. Section VI discusses the possible exploitation scenarios. Finally, Section VII provides our concluding remarks and future works.

II. Related Work

When dealing with pure software power systems' models and simulators, different solutions are proposing co-simulation technologies to interconnect heterogeneous simulation environments by means of an orchestrator entity that manages time evolution, regulation, and data exchange between different simulator entities. For instance, Bharati et al. [11] implement a complex transmission and distribution co-simulation framework based on HELICS to effectively provide innovative algorithms for future power grid planning, validation of controls under critical contingencies, and validation of various wide-area monitoring and controls. However, these solutions cannot deal with the time-domain analysis (e.g. EMT) of large AC power systems that requires significant computational power to reduce the simulation time-step, enlarge network sizes, and accurately capture the fast transients. For EMT analysis, a widely accepted and well used pure software solution is the Electro-Magnetic Transients Program (EMTP) [12] that implements the Dommel algorithm for the network solution.

The requirements for real-time simulation make it necessary to exploit a parallel computing architecture. Different works analysed multi Digital Signal Processor (multi-DSP) [13]–[15], multi Reduced Instruction Set Computer (multi-RISC) [16], PC-cluster architectures [17], [18] and FPGA solutions. For instance, Chen et al. [19] present an FPGA-based real-time EMTP simulator based on a deeply pipelined paralleled Dommel algorithm.

In the last decades, different commercial real-time power network simulators have gained the interest of power system designers to address the real-time constraint and apply PHIL testing. The most important DRTS producers for power system analysis are RTDS Technology and Opal-RT. In particular, RTDS Technology proposes the NovaCor chassis, a POWER8 RISC 10-core architecture, capable of continuous real-time EMT. Different plug-and-play external boards enable Digital I/O, Analogue I/O, and standard communication protocols for power systems (e.g. PMU, GOOSE, SV, MODBUS, etc.) according to Standards IEEE C37.118 [20] and IEC 61850 [21], widening its scope of application. Finally, RTDS provides RSCAD, a comprehensive software to design complex power system scenarios. However, RTDS suffers a limited number of nodes that restricts the scalability of the PSUT. Different works have proposed to relax the complexity of the simulation of some parts of the power network in analysis and scale up the PSUT, the so-called multi-rate approach [22]. The multi-rate approach proposes to define different time resolutions for different areas of the PSUT but still, the scalability is limited.

To cope with such a limitation, the power system research community starts proposing to interconnect together different DRTS exploiting fast high-bandwidth telecommunication protocols based either on TCP or UDP. A detailed overview of methods, test procedures, studies, and experiences in this regard is provided in [23]. This work is presented by members of the Survey of Smart Grid International Research Facility Network task on Advanced Laboratory Testing Methods. Other related co-simulation works are discussed in [24], [25] for distribution networks and Transmission System Operator (TSO)-Distribution System Operator (DSO) customer coordination studies, respectively.

For instance, the VILLAS framework [26] allows the setup of geographically distributed laboratories, interconnecting different DRTS to enable PHIL testing. But even with these optimistic premises, DRTS interconnection suffers a series of inaccuracies due to time latencies, jitter, limited bandwidth, and network interface management of the communication link. These inaccuracies could affect the stability of a PSUT co-simulation as in PHIL systems when trying to interconnect a DUT to a simulated ROS. In fact, PHIL introduces several criticalities with error (i.e. time delay and power amplifier harmonics distortion) generated by the power interface that may cause severe instability issues or unacceptably inaccurate results. These effects are comparable to DRTS interconnection ones. Similarly, [27] presents a framework for virtual integration of laboratories. This can enable co-simulation and joint experiments involving both hardware and software resources hosted at geographically distributed laboratories. In [28], Ren et al. present the PHIL instability problem highlighting the importance of checking the closed-loop stability and improving it through a particular IA. In [5], the most interesting IA are compared together: *i)* the ITM and its variants [29]–[31], and *ii)* the Damping Impedance Method with different estimation algorithms of the damping impedance [32], [33]. The outcome of this comparison highlights that ITM is the straightforward and the simplest IA to implement PHIL application.

More general Hardware-In-the-Loop (HIL) interconnection for Intelligent Electronic Device (IED) testing (e.g. PMU) could exploit other ICT to mitigate the effects of desynchronisation among DRTS internal clock and the IED DUT in HIL configuration. In this regard, IEEE1588 PTP [9] is one of the most used synchronisation protocols in Smart Grid testing. PTP aligns with high precision different internal clocks avoiding effects of time misalignment of ROS and DUT during real-time simulations. For instance, Blair et al. [34] propose a real-time test-bed for measurements and analysis of distributed PMU systems for Smart Grid control and protection exploiting PTP to synchronise the simulated ROS and the PMU IED DUT. Similarly, a co-simulation test bench using

OPAL-RT with its modelling software RT-LAB and FPGAs for analysing photovoltaic power generation systems is presented and discussed in [35]. EMT-Root Mean Square (RMS) co-simulation involving Opal-RT's ePhasorSim and RTDS is covered in [36]. This work demonstrates the applicability of this co-simulation for HIL testing of protective relays. Likewise, [37] presents a hybrid co-simulation setup based on the Mosaik framework for EMT-RMS co-simulations. In this work, the authors employ the Functional Mock-up Interface (FMI) for the co-simulations. Power systems and communication co-simulations are discussed in [38]–[40] for SCADA systems, cyber-physical studies, and cybersecurity investigations, respectively.

None of the above-mentioned methodologies in literature is capable of enhancing the PSUT scalability in a co-simulation framework for pure EMT analysis with similar performances in terms of stability and accuracy of the numerical solution. The proposed Distributed Digital Real-Time Co-simulation Infrastructure instead applies Aurora 8B/10B, the fastest communication protocol on DRTS boards. It ensures the lowest communication latency, consequently the lowest non-linear effect on the PSUT numerical solution. With respect to our previous work [10], the proposed co-simulation architecture interconnects two physical DRTS (i.e. RTDS NovaCor) by exploiting IEEE1588 PTP to synchronise and regulate time evolution with high precision by aligning internal reference clocks of the different DRTS interconnected with the GPS clock signal. The proposed architecture innovate the DRTS co-simulation state-of-the-art by: *i)* implementing an homogeneous co-simulation framework that allows the scalability of the PSUT also in fast time-stepped analysis, such as pure EMT ones; *ii)* interconnecting locally distributed DRTS exploiting an on-site co-simulation approach, such as an optical fiber link that ensures the lowest latency among the different DRTS; and, finally, *iii)* ensuring a real-time co-simulation infrastructure to enable PHIL tests. The proposed hybrid co-simulation infrastructure applies the theory of PHIL applications. In fact, another novelty proposed in this paper is the application of the ITM IA to split the PSUT into two subsystems that will be distributed among the involved DRTS. Exploiting ITM IA, we can obtain the decoupled PSUT numerical solution. This is demonstrated by following the Nyquist principles of frequency-domain analysis commonly used in the PHIL context to determine the stability of IA. Furthermore, the application of the fastest communication protocol ensures the lowest communication latency, ensuring the lowest non-linear effect on the PSUT numerical solution originated by the ITM IA application. The proposed frequency-domain and time-domain analysis fund the basis for the application of co-simulation infrastructure in power system analysis.

III. Technological Background

Co-simulation is a flexible approach to integrating different domain-specific simulators in a shared and distributed simulation environment. Following this paradigm, a complex scenario is decomposed in a system of systems topology in which each node (i.e. subsystem) is simulated by a different simulator engine (or solver). This decomposition allows choosing among a set of domain-specific simulation tools to find the best solution that enhances numerical calculation and boosts the computational time of a single subsystem. For instance, DRTS is a plus to fulfil a Smart Grid simulation in a distributed co-simulation infrastructure.

The co-simulation approach must preserve high efficiency and accuracy in each single subsystem simulation. Furthermore, the complex dynamic system of systems simulation obtained by coupling different simulators may not cause instability and inaccuracies. In fact, computer-aided power system analysis with DRTS could be error-prone in a co-simulation environment. The effect of interconnecting different DRTS together could lead to results that differ from a standalone simulation, affecting the numerical stability and accuracy of the solution. The main challenges in this regard are Time Synchronisation and Regulation, and Communication.

Time Synchronisation is mandatory when the distributed co-simulation infrastructure interacts in a time-dependent manner. It refers to the algorithm used to ensure temporally correct ordering among events generated by various simulators. *Time Regulation* instead refers to the need of instituting a policy to regulate how individual simulators evolve time. For instance, a particular simulator could be the leader of the distributed environment (i.e. time-regulating), some others could be a follower (i.e. time-constrained). Depending on the application, a policy must be created using a correct time regulation scheme for the simulators involved, which can have a major impact on the performance and correctness of the distributed co-simulation environment.

Time Synchronisation and Regulation issues could be neglected by choosing the right time regulation schema and synchronising the starting point of each subsystem simulation. In the real-time world, each DRTS normally manages time evolution independently to fulfil its real-time constraint and cannot be controlled from an external source. So, the best time regulation schema is setting all nodes as time-regulating ones. The evolution in time is ensured by considering each DRTS independent of each other and following the same wall clock time. Synchronisation instead is important to run specific PSUT that require precise phase relationships among generators in the separate subsystems. This task is ensured by the application of network time protocols (e.g. IEEE1588 PTP) that align internal DRTS clocks and run each subsystem with a common wall clock starting time.

On the other hand, *Communication* refers to data exchange among different interconnected simulators, normally carried out by telecommunication protocols. Choosing the right protocol is fundamental to designing an accurate and reliable co-simulation infrastructure, capable of ensuring the stability of the numerical solution. The main issues are normally generated by latency (or lag). In a co-simulation context, latency is the time delay between the sending procedure of data retrieved from a simulator engine and the receiving procedure that provides the received data to the solver of other distributed simulator environments to fulfil their numerical calculation. Latency is the main cause of instability and inaccuracies for a distributed co-simulation infrastructure and must be mitigated

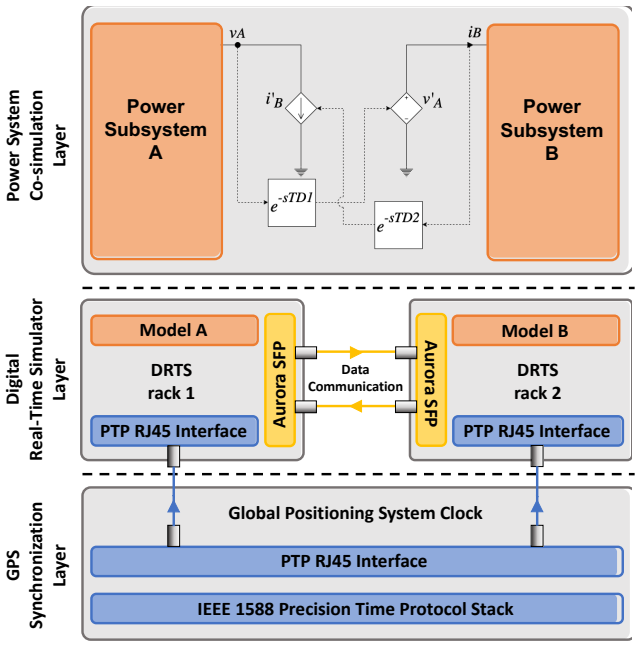

Fig. 1. The Digital Real-Time Co-simulation Infrastructure and its three main architectural layers.

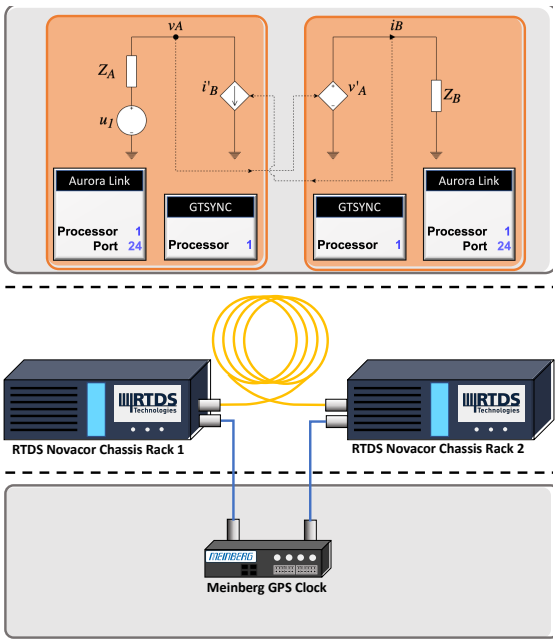

Fig. 2. The RTDS NovaCor co-simulation laboratory setup exploiting the Digital Real-Time Co-simulation Infrastructure.

by applying specific techniques.

IV. Methodology

Communication strongly affects the numerical stability of DRTS co-simulation infrastructures introducing latency due to telecommunication protocols that are normally used to apply co-simulation techniques (e.g. TCP and UDP). To reduce the latency effect on the numerical solution of a co-simulated PSUT, we propose the Digital Real-Time Co-simulation Infrastructure described in Figure 1. The infrastructure is composed of three main layers, namely, *i)* the *GPS Synchronization Layer*, *ii)* the *Digital Real-Time Simulator Layer*, and *iii)* the *Power System Co-simulation Layer*.

The *Digital Real-Time Simulator Layer* is the core layer of the proposed infrastructure that allows a bi-directional point-to-point physical interconnection between two different DRTS. The involved DRTS must meet two main requirements: *i)* supporting Aurora 8B/10B protocol with Small-form Factor Pluggable (SFP) interfaces to allow data communication between simulators, and *ii)* providing a synchronisation board to implement the IEEE1588 PTP protocol stack with an RJ45 interface to synchronise the internal reference clocks with the underlying layer. The first requirement allows the exploitation of the Aurora 8B/10B protocol that is a high-performance lightweight link-layer protocol developed by Xilinx to exchange data across a point-to-point standard full-duplex multimode optical fiber link, ensuring a low communication latency. The Aurora implementation in the proposed infrastructure chooses a single 2-width lane with a framing interface capable of reaching a line rate of 2Gbps with a duplex communication without flow control. The frame is completely configured by the end-user choosing a variable sequence of integer and 32-bit float. Apart from data formats, it has no particular restrictions. The Aurora protocol ensures the lowest latency between the communication protocols available on-board for the interconnection between DRTSs. The second requirement instead enables the management of the time synchronisation schema among DRTSs by exploiting the IEEE1588-2008v2 PTP Default Layer 2 stack in both End-to-End (E2E) and Peer-to-Peer (P2P) configurations. The IEEE1588 PTP protocol permits the alignment of the DRTS internal reference clock with a precision of tens of nanoseconds, depending on the master node implementation managed by *GPS Synchronization Layer*.

The *GPS Synchronization Layer* implements the IEEE1588 PTP master node by exploiting a GPS clock that uses the GPS signal to synchronize its internal reference clock with the GPS atomic clock technology. It provides the infrastructure with access to the atomic time standards without needing a local atomic clock, ensuring a global synchronization. Concerning the time regulation schema, it can be neglected since the DRTS racks evolve their simulation with an independent time-regulating schema that ensures the correct event ordering respecting the proper real-time constraint of DRTS. Since the proposed circuit to test the interconnection is a simple source-load circuit, the source part will trigger the simulation starting time of the load. Results from the different DRTS racks are indeed aligned considering the internal clock time as a reference since the IEEE1588 PTP stack ensure the correct time synchronisation schema.

Finally, the *Power System Co-simulation Layer* allows splitting a PSUT into two power subsystems by exploiting the ITM IA described in Figure 3. This IA, normally applied to PHIL application, exploits a controlled voltage generator in the subsystem B of the circuit that reproduces the voltage v_A measured in the subsystem A (i.e. v'_A), and a current generator in the subsystem A of the circuit to reproduce the current i_B measured in the subsystem B (i.e. i'_B). Moreover, it applies

a latency that is proportional to the latency experimented by the exchanged variable from DRTS rack 1 to DRTS rack 2 to take effect on the subsystem B circuit (i.e. T_{D_1}) and vice versa (i.e. T_{D_2}).

The rest of this section introduces *i)* the laboratory setup of the proposed co-simulation infrastructure, and *ii)* the frequency stability analysis of the ITM IA that has been applied on a simple electric test case. The split test case has been then applied to assess both time- and frequency-domain accuracy analyses of proposed infrastructure.

A. Laboratory Setup

The laboratory setup proposed in Figure 2 implements the Digital Real-Time Simulator Layer of the proposed infrastructure by interconnecting two RTDS NovaCor racks exploiting the Aurora 8B/10B protocol. In particular, they are connected with a 25 meters optical fiber link by exploiting the SFP port 24 in each rack. Aurora could be enabled in both RSCAD drafts by using the *_rtds_aurora* block, the so-called *Aurora block*. This block allows defining the selected SFP transceiver port, the processor number, a priority level of computation, the frame definition (i.e. exchanged environment variables) and the sequence number blocking property of the Aurora link. More in-depth on sequence number blocking activation, it minimises the loop delay between the communicating RTDS NovaCor racks. In fact, the sequence number is a counter that is always appended to each frame. Once the sequence number blocking property is activated, each rack must take the sequence number it receives and echo it back at the end of the response frame that is sent back to the sender and vice versa. The response of the echoed answer with the received sequence number must be fairly quick and less than the fixed simulation time step. Since a one-way communication latency takes only 1100 ns in the RTDS NovaCor rack, this restriction is always respected.

However, latency in the numerical solution varies in respect to this value due to the complex Power8 RISC 10-core architecture implemented in RTDS NovaCor racks. In fact, the most significant latency components are caused by the variables exchanged between control signals core and network solution cores. Control signal core is in charge of managing control variables, like data received from Aurora. Network solution cores instead solve the differential equation of the proposed PSUT applying network variables (i.e. voltages and currents) to the impedance matrix of the system. Several simulation time steps could be required to pass through control variables from control core to network variables in the network solution core. In the end, the proposed co-simulation infrastructure allows a precise calculation of the latency generated by the overall communication process, not only the telecommunication protocol one.

The time synchronisation schema among the RTDS NovaCor racks is achieved through IEEE1588 PTP by interconnecting each DRTS synchronization board with the GPS Synchronization Layer, allowing a fine alignment of the internal clocks of each DRTS. In our infrastructure, RTDS NovaCor racks must be provided with GTSYNC card capability to manage the interaction with the IEEE1588 PTP stack. GTSYNC is

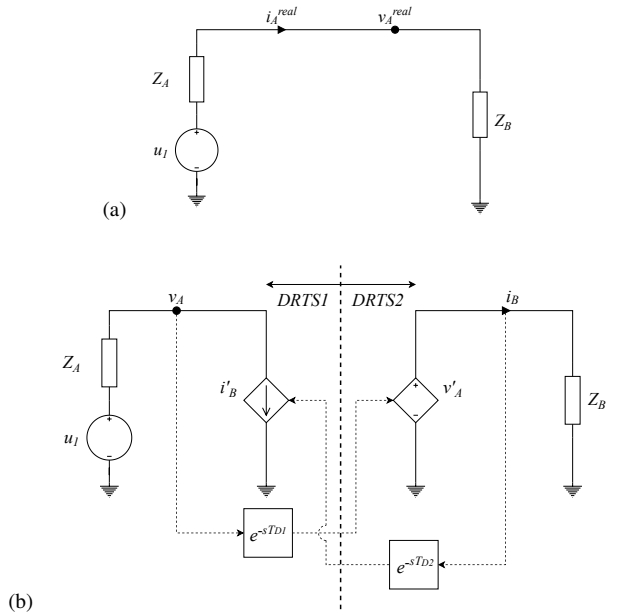

Fig. 3. Monolithic electric circuit (a) composed by an AC voltage source u_1 and two impedances Z_A and Z_B and the application of ITM IA (b)

a peripheral board interconnected with an RTDS NovaCor rack by means of an optical fiber link that allows different kinds of synchronisation protocols (e.g. IEEE1588 PTP, 1PPS, IRIG-B) both in slave and master mode. To enable GTSYNC capabilities in the RTDS NovaCor rack, the GTSYNC block must be added in the RSCAD draft of the simulated use case. In Figure 2, the RTDS NovaCor racks are interconnected with the Meinberg microSync HR102HQ GPS clock through an Ethernet Copper RJ45 cable. The IEEE1588 PTP profile is an IEEE1588-2008v2 Default Layer 2 with a P2P Transparent Clock (TC), mandatory for GTSYNC communication. Obviously, the Meinberg microSync HR102HQ GPS clock is set as the master node of the IEEE1588 PTP stack, and the two GTSYNC cards of the RTDS NovaCor racks are set as slaves to ensure a proper setup of the synchronisation with the reference GPS clock.

B. ITM IA Frequency Stability Analysis

Communication latency is normally experimented in PHIL applications with similar effects to co-simulation applications. In the PHIL context, a monolithic electric system (see Figure 3a) is split into a real hardware DUT and a simulated ROS. However, the splitting is not ideal because the power interface (i.e. power amplifier) and the sensors to retrieve real measurements between ROS and DUT may experience delays and errors (e.g. offset, harmonics distortion, nonlinearities, etc.). Specific techniques must be applied to ensure stability and accuracy of the overall PHIL system, the so-called Interface Algorithm (IA). In particular, the Ideal Transformer Method (ITM) described in Figure 3b is the simplest way to set up a PHIL system.

In Figure 4, the equivalent block diagram of the ITM circuit could lead us to its frequency-domain stability analysis. Exploiting the ITM open-loop function described by Equation 1, the Nyquist diagram is calculated for $Z_A = 50\ \Omega$

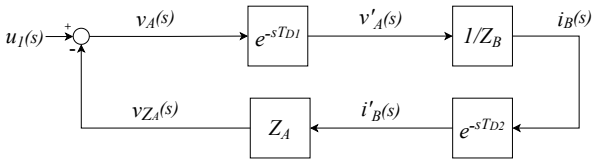

Fig. 4. Equivalent Block Diagram of the ITM IA

and different values of Z_B, namely $50, 100, 200, 300, 400$, and $500\,\Omega$. Following the Nyquist criterion, the Nyquist diagram of the open-loop function of the ITM system must not encircle the critical point $(-1, 0)$ to ensure stability. As depicted in Figure 5, the ratio Z_A/Z_B must be minor than 1 to ensure the Nyquist criterion. Also if the stability is ensured by this criterion, a large latency of the paths T_{D_1} and T_{D_2} could provoke nonlinearities (i.e. phase shift) that impact both frequency-domain and time-domain accuracy of the overall system.

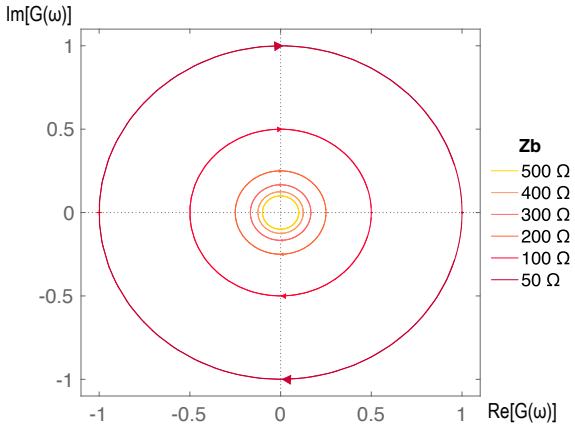

Fig. 5. Nyquist diagrams of the open-loop transfer function G_{ol}

$$G_{ol} = \frac{Z_A}{Z_B} e^{-s(T_{D_1}+T_{D_2})} \tag{1}$$

One of the novelties proposed in this work is the application of the ITM IA to the Digital Real-Time Co-simulation Infrastructure. Indeed, the ITM IA can be applied also in the DRTS interconnection to split a PSUT into two subsystems, as depicted in the Power System Co-simulation Layer in Figure 1. In particular, the ITM IA has been applied to the simple electric circuit in Figure 3a. The Power System Co-simulation Layer of the proposed experiment in Figure 2 reproduces the ITM circuit in Figure 3b modelling each of the two subsystems in a different RSCAD draft, representing subsystems A and B of the general infrastructure. The Aurora blocks enable the Aurora protocol data communication between the two DRTSs by setting for each draft *i)* the SFP to port 24, *ii)* the processor number (i.e. Processor 1 in our tests), and *iii)* a high priority of the Aurora block. Then, the GTSYNC block has been included in both drafts to enable the synchronisation of each RTDS NovaCor with the GPS clock.

V. Analysis of Numerical Stability and Accuracy

In the following section, two different experiments are described: *i)* Communication Latency Calculation, and *ii)* ITM IA application. Afterwards, both time-domain and frequency-domain accuracy analyses are conducted over the results obtained by the ITM IA application.

A. Communication Latency Calculation

The communication latency calculation has been carried out by exchanging a reference clock through the Aurora link to calculate the difference with the receiving simulation time. The reference clock has been sent from 2 to 128 times for each simulation time step, which are the minimum and maximum values allowed to be exchanged following the specification of the RSCAD Aurora block. This setup has been repeated for different time step duration T_{Sim} from $5\,\mu s$ to $500\,\mu s$.

Latency results 0 for all T_{Sim} values and all number of variables exchanged, confirming the setup of the co-simulation infrastructure described in Section IV-A. However, they cannot be considered as a reference latency for a co-simulated electric grid use case. In fact, clock variables exchanged in this simple testbed belongs to the control signal core of the RTDS NovaCor racks. Vice versa, voltage and current variables of an electric use case belong to network solution cores. As mentioned in Section IV, the RTDS NovaCor architecture implements a complex parallelization of the computation required for the network solution and the control signals management. This results in a variable latency to move a network variable from a network solution core to the control signal core, and vice versa.

Moreover, the latency varies depending on the exchanged variable type (i.e. voltages or currents) due to simulation blocks implementation composing the electric use case. Considering the ITM circuit, voltage variables are exchanged from the network solution core to the control signal core of RTDS NovaCor rack 1 and then sent through the Aurora link to RTDS NovaCor rack 2. There is where they are received by the control signal core and exchanged from the control signal core to the network signal core. This task requires $3T_{Sim}$ to impact the network solution of the RTDS NovaCor rack 2 for all T_{Sim}. Vice versa, the backward path of the current variables from RTDS NovaCor rack 2 to rack 1 takes only $2T_{Sim}$.

B. ITM IA Application

The ITM circuit described in Figure 3b has been reproduced in RSCAD software by splitting the source and the load part among the two RTDS NovaCor racks. In rack 1, the sinusoidal voltage source u_1 has been configured with a voltage magnitude of $100\,kV$ peak and a frequency of $50\,Hz$. Moreover, the pure resistive impedance Z_A has been fixed to $50\,\Omega$. A metering point v_A is set to retrieve the voltage and will allow exporting the network variable to the control core of rack 1. This operation will take $1T_{Sim}$. For each time step, the exported control variable v_A is sent through the Aurora link on port 24 of rack 1 and received by the control core of rack 2 on port 24. As previously demonstrated by the test in Section V-A, this operation takes no time step. On rack 2, the control variable received v'_A is imported into the network solution core and forces the controlled voltage source to generate v_A. This operation will take $2T_{Sim}$. The

total latency for sending v_A to the right part of the circuit is therefore $3T_{Sim}$.

In rack 2, Z_B is set to two different values, respectively *i)* $50.5\,\Omega$ to test the ITM near the instability region, and *ii)* $500\,\Omega$ to present a stable ITM IA application. The current i_B flowing into the impedance Z_B is then exported to the control core, sent through Aurora from port 24 to port 24 of rack 1, and then applied to the controlled current source to generate i'_B. As the controlled current source requires only $1T_{Sim}$ to fulfil the operation of exchanging the received Aurora variable from the control core to the network variable i'_B , this operation takes in total $2T_{Sim}$. So, the complete round-trip latency results in $5T_{Sim}$.

The time step duration T_{Sim} has been changed from $50\,\mu s$ to $500\,\mu s$ to run different tests and analyse voltages v_A, v_B and currents i_A, i_B for the two Z_B values. The monolithic electric circuit in Figure 3a has been run simultaneously to the ITM case on rack 1 in order to retrieve the correct voltages and currents, namely v_A^{real} and i_A^{real}. The test results demonstrate that applying a T_{Sim} lower than $500\,\mu s$ ensures good time-accuracy results. The results presented in the next sections are obtained for the worst-case scenario, that is when T_{Sim} is set to $500\,\mu s$, and the average case scenario, with a T_{Sim} equal to $50\,\mu s$ (i.e. standard EMT analysis). The results are presented only for voltages to avoid repetition, as the power factor of a purely resistive circuit is 1 and currents and voltages are in phase.

C. Time-domain Accuracy Analysis

1) Worst-Case Scenario ($T_{Sim} = 500\ \mu s$): The worst-case scenario is considered as a limit case, as normal EMT analysis in power systems studies are usually performed with much smaller time steps, and usually $T_s \approx 50\,\mu s$. The purpose of this analysis is to reach the limit of the latency non-linear effect on the co-simulated ITM circuit.

Results of ITM IA voltages are compared with the monolithic electric circuit solution for both Z_B values to assess a quantitative time-domain accuracy of the numerical solution. The case $Z_B = 500\ \Omega$ is presented in Figure 6a. v_A (*green line*) is overlying v_A^{real} (*blue line*) confirming that the calculations in both cases are comparable with a 2.28% rise of the v_A voltage peak due to the latency experimented by i_B to be reflected on the left part of the ITM circuit. v_B (*orange line*) instead correctly presents a latency of $1500\,\mu s$ that is equal to $3T_{Sim}$. v_B also experiences a rise in respect to v_A^{real} following v_A trend.

The case $Z_B = 50.5\ \Omega$ in Figure 6b instead presents major voltage distortion. In fact, v_A presents a distortion transient that is a direct effect of the phase shift due to the round trip latency of the ITM application, equal to $5T_{Sim}$, and also of the magnitude of Z_A/Z_B equal to $0.\overline{9900}$. The initial peak of the distortion exceeds 40% in respect to v_A^{real}. v_B clearly follows the same v_A trend with a latency of $1500\,\mu s$ that is equal to $3T_{Sim}$. Moreover, the distortion transient presented in Figure 7 gets absorbed in $0.4\,s$ stabilising the result with a 7.92% rise in respect to the voltage arising of the case $Z_B = 500\ \Omega$. Furthermore, distortion can be appreciated due to the effect of the phase shift generated by the identified latency.

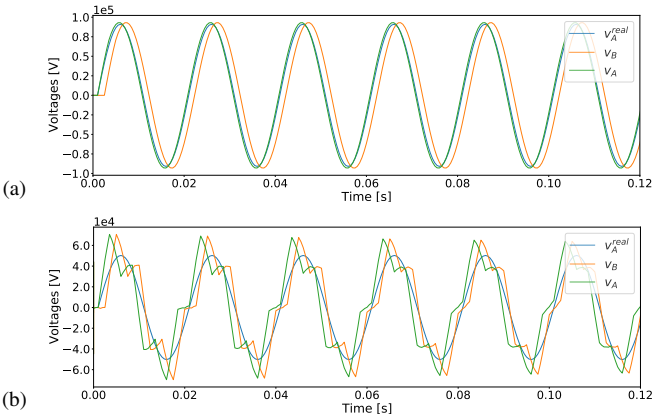

Fig. 6. Voltages time plots to compare time-domain accuracy of the monolithic circuit (*blue*) and ITM IA application (blue) for $T_s = 500\,\mu s$ (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

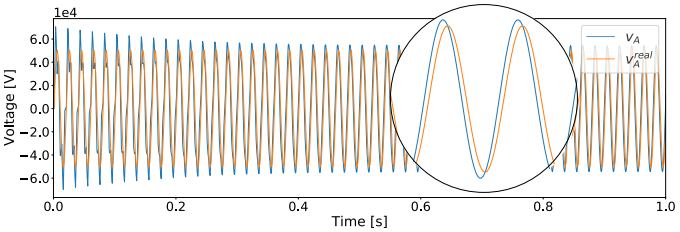

Fig. 7. Voltages time plots of the transient when applying ITM IA for $T_s = 500\,\mu s$ near the instability region $Z_B = 50.5\ \Omega$ and its non linear effect on the numerical solution

2) Average Case Scenario ($T_{Sim} = 50\ \mu s$): The average case scenario is considered as a normal EMT analysis case for a general electric grid scenario. The purpose of this analysis is to evaluate the goodness of the stability and accuracy of the co-simulated ITM circuit, demonstrated by the comparison with results of the worst-case scenario in Section V-C1. Also for the average case, results are compared with the monolithic electric circuit solution for both Z_B values, as described in Section V-C1.

The case when $Z_B = 500\ \Omega$ is presented in Figure 8a. v_A (*green line*) is overlying v_A^{real} (*blue line*) with an irrelevant increase of 0.023% of the v_A voltage peak due to the small latency experimented by i_B to be reflected on the left part of the ITM circuit. v_B (*orange line*) instead correctly presents a latency of $150\,\mu s$ that is equal to $3T_{Sim}$. v_B also experiences an irrelevant increase in respect to v_A^{real} following v_A trend.

The case when $Z_B = 50.5\ \Omega$ in Figure 8b instead presents a minor voltage distortion with respect to the worst-case scenario. In fact, the amplitude of the distortion transient is lower and it expires rapidly. The initial peak of the distortion exceeds 3.23% in respect to v_A^{real}. v_B follows the same v_A trend as in the previous case with a latency of $150\,\mu s$ that is equal to $3T_{Sim}$. Moreover, the distortion transient presented in Figure 9 gets absorbed in $0.04\,s$ stabilising the result with an irrelevant rise of 0.074% of v_A voltage in respect to v_A^{real}. No distortion or non-linearity can be appreciated due to the phase shift generated by the identified latency. Further insights on the topic will follow in the frequency-domain accuracy analysis.

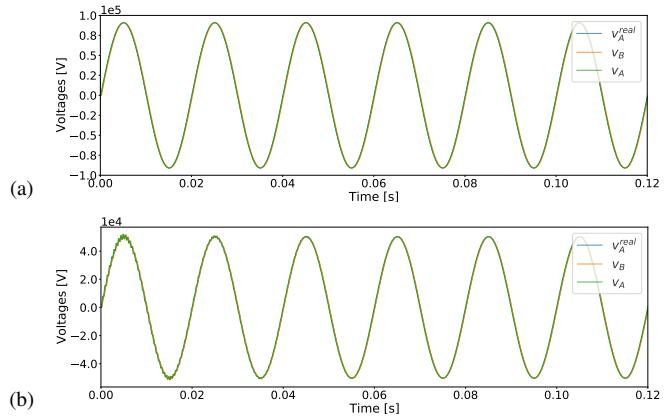

Fig. 8. Voltages time plots to compare time-domain accuracy of the monolithic circuit (*blue*) and ITM IA application (blue) for $T_s = 50\,\mu s$ (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

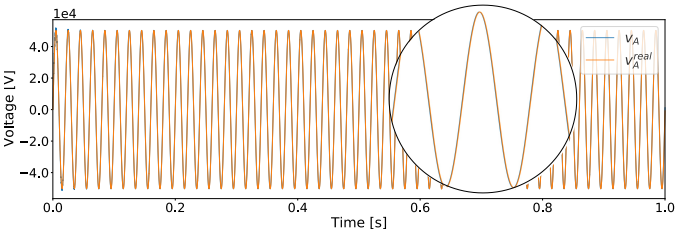

Fig. 9. Voltages time plots of the transient when applying ITM IA for $T_s = 50\,\mu s$ near the instability region $Z_B = 50.5\ \Omega$

D. Frequency-domain Accuracy Analysis

1) Worst-Case Scenario ($T_{Sim} = 500\ \mu s$): The frequency-domain accuracy analysis is obtained applying Welch's method for the Power Spectral Density (PSD) estimation to obtain a frequency description of the voltage signals for both Z_B values. For $Z_B = 500\ \Omega$, v_A PSD is overlying the v_A^{real} peak at $f = 50\,Hz$, that is the power supply frequency. Thus, the frequency content representation of the sine is correctly replicated as depicted in Figure 10a. The case $Z_B = 50.5\ \Omega$ instead presents three different frequency peaks at $f = 200$, 600 and $1000\,Hz$ as well as the former peak at $f = 50\,Hz$. The phase shift time-domain effect is similar to a triangle wave trend. A triangle wave can be approximated in time-domain with additive synthesis, summing odd harmonics of the fundamental sine wave of frequency f_Δ while multiplying every other odd harmonics by -1 and multiplying the amplitude of the harmonics by one over the square of their mode number n as described in Equation 2:

$$x_{triangle}(t) = \frac{8}{\pi^2} \sum_{i=0}^{N-1} (-1)^i n^{-2} sin(2\pi f_\Delta n t) \tag{2}$$

As for each $5T_{Sim}$ the phase shift time-domain effect changes signs, we can consider the fundamental sine wave period of the generated triangle wave T_Δ twice the round trip latency, resulting $10T_{Sim}$. The fundamental frequency f_Δ is equal to the inverse of the period T_Δ. As T_Δ is equal to $10T_{Sim}$, the fundamental frequency f_Δ is equal to $200\,Hz$, confirming the empirical results. Consequently, the frequencies

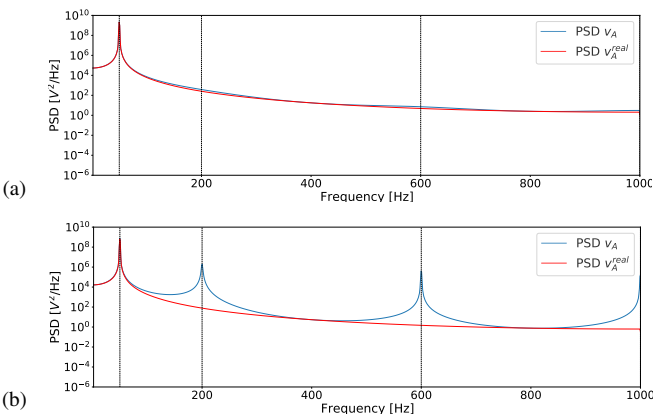

Fig. 10. Voltages Power Spectral Density (PSD) estimation applying Welch's method to compare frequency-domain accuracy of the monolithic circuit (*red*) and ITM IA application for $T_s = 500\,\mu s$ (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

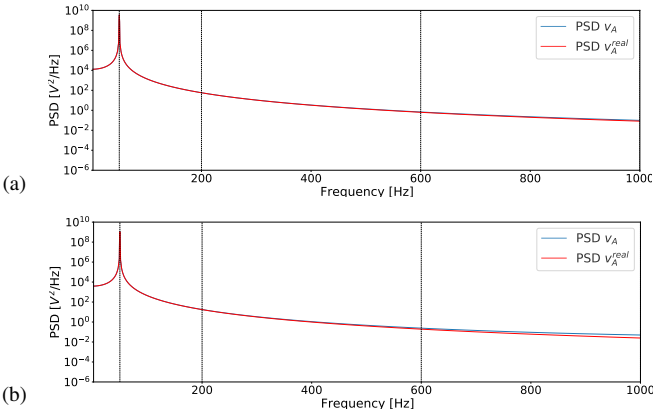

Fig. 11. Voltages Power Spectral Density (PSD) estimation applying Welch's method to compare frequency-domain accuracy of the monolithic circuit (*red*) and ITM IA application for $T_s = 50\,\mu s$ (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

of the odd harmonics are $600\,Hz$, $1000\,Hz$, and so on. This effect can be noticed clearly also for $Z_B = 500\ \Omega$ but it is mitigated by the magnitude of Z_A/Z_B equal to 0.1.

2) Average Case Scenario ($T_{Sim} = 50\ \mu s$): Like in the worst-case scenario, Welch's method for the PSD estimation is applied to the results for both Z_B values.

For $Z_B = 500\ \Omega$, v_A PSD is overlying the v_A^{real} peak at $f = 50\,Hz$ without appreciable distortions, like in the worst-case scenario. This result can be appreciated in Figure 11a. The case $Z_B = 50.5\ \Omega$ still overlays the v_A voltage signal PSD with the v_A^{real} voltage signal PSD with a former peak at $f = 50\,Hz$ as presented in Figure 11b, differently from the worst-case scenario. However, it can be appreciated a slight rise in the frequency peaks at $f = 200$, 600 and $1000\,Hz$, as in the worst-case scenario. This effect is due to the non-linearity generated by the latency phase shift experimented during the initial transient in Figure 9. This confirms the latency calculated and its superimposed triangle wave effect that modifies the initial transients of v_A and v_B with respect to v_A^{real}.

Finally, Table I resumes all the experimental results pre-

T_{Sim} [µs]	Z_B [Ω]	v_A Initial Over Peak [%]	v_A Asymptotic Over Peak [%]	v_A Transient Duration [s]	f_Δ [Hz]
50	500	0.023%	0.023%	-	-
	50.5	3.23%	0.074%	0.04	2000
100	500	0.092%	0.092%	-	-
	50.5	7,20%	0,29%	0.08	1000
500	500	2.28%	2.28%	-	-
	50.5	40.01%	7.92%	0.4	200

TABLE I
COMPARISON OF RESULTS FOR DIFFERENT TIME STEP DURATIONS

sented in this section. Since larger PSUT could require higher time step duration to avoid overruns and time step overflows on a single DRTS rack, an additional test-case is reported with $T_{Sim} = 100\,\mu s$. This additional test demonstrates that results are comparable also with a larger time step duration with a low rise of the key performance indexes obtained by the *Average Case Scenario* (i.e. $T_{Sim} = 50\,\mu s$).

VI. Discussion on Possible Exploitation

The co-simulation infrastructure presented in this paper could be applied for the analysis of different case studies, such as:

1) Simulation of large transmission and distribution networks, in which the two subsystems are simulated in two different DRTSs. In this way the equivalent impedance ratio between the two systems can guarantee stability and large systems can be simulated, thanks to the coupling of the computation power of the two DRTSs.
2) Simulation of power electronics devices coupled to a smart grid, in which the power electronic devices are modelled in detail in one DRTS, with a very small time step duration, while the smart grid is modelled in the second DRTS. Thanks to the decoupling, a different time step duration can be used and a larger system can be simulated in the second DRTS.
3) Simulation of a large distribution network on one simulator, (e.g. in RTDS the distribution mode could be used) coupled with a LV microgrid modeled in detail in pure EMT. Also in this case the equivalent impedance ratio between the two systems can guarantee stability and large systems can be simulated, thanks to the coupling of the computation power of the two real-time simulators.

VII. Conclusion

A stability and accuracy analysis of the infrastructure proposed to interconnect DRTS for co-simulation was presented. Similarly to what happens in a PHIL setup, the application of the ITM IA to DRTS interconnection ensures stability and accuracy of the numerical solution of a PSUT with the constraint: $Z_A/Z_B << 1$. The adoption of the Aurora protocol for communication helps reduce latency and therefore improves stability and accuracy. In our previous work, a single DRTS with an Aurora echo link was implemented to avoid complex time synchronisation schema and virtually test the proposed infrastructure. The proposed infrastructure instead implements an innovative time synchronisation schema applying IEEE1588 PTP to align results coming from both DRTS interconnected. A worst-case scenario with a simulation time step of $500\,\mu s$ has been analysed to assess the time-domain accuracy of the solution in both stability and near the instability regions. The ITM IA application ensures in both cases an acceptable accuracy in reproducing the behaviour of the monolithic electric circuit. With respect to our previous work, in this paper, we presented an average case scenario with a time step of $50\,\mu s$ to demonstrate that the proposed infrastructure is accurate and stable both in time-domain accuracy and frequency-domain stability. As EMT analysis commonly uses a time step duration similar to the average case scenario (i.e. around $50\,\mu s$), we can assume that we can exploit the ITM IA in DRTS interconnection to ensure numerical stability. Moreover, a smaller time step also allows for a relaxation of the constraint related to the impedance ratio, making it possible to operate with $Z_A/Z_B \approx 1$. However, our infrastructure and the ITM IA application suffers from different limitations: *i)* it only allows point-to-point interconnection. To overcome this limit, the same DRTS can establish different point-to-point communications with other simulators, creating a mesh topology. Nevertheless, DRTS have a limited number of Aurora SFP ports, thus a limited number of point-to-point interconnections, which limits the scalability of our infrastructure; *ii)* the optical fiber link required for Aurora protocol limits the maximum distance between the interconnected DRTS; *iii)* it does not allow geographically distributed laboratory interconnection but only local ones, enabling faster co-simulation scenario (e.g. EMT analysis); *iv)* finally, the ITM IA offers a limited stable solution state space. Other IA could be analysed to ensure higher stable solution state space, such as Phasor Domain and Wave Transformation. Future work will include other PHIL IA (e.g. Phasor Domain or Wave Transformation) to extend the stable solution state space of a PSUT and interconnecting different types of DRTS (e.g. RTDS, OPAL-RT, and hybrid interconnections) in order to expand the computational capabilities of individual laboratories, exploiting Aurora 8B/10B protocol and the synchronisation capabilities of the IEEE1588 PTP.

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