Stability and Accuracy Analysis of Digital Real-Time Simulator Interconnection for Co-simulation Infrastructure Design

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***Abstract*—Co-simulation techniques are gaining popularity among power system research community to analyse future scalable Smart Grid solution. However, complicancy due to co-simulation application such as communication protocol latency uncertainty are holding-up the widespread usage of these techniques in power sytstem analysis. These issues impact more when dealing with Digital Real-Time Simulation (DRTS) for the strict real-time constraint introduced to test Power Hardware-In-the-Loop (PHIL). In this paper, an innovative co-simulation infrastructure allows to interconnect different DRTS exploiting Aurora 8B/10B protocol to reduce the effects of communication latency and respect real-time constraint. Moreover, Ideal Transformer Method Interface Algorithm (ITM IA) is applied to the DRTS interconnection. This IA, commonly used in PHIL application, enhances stability and accuracy of the numerical solution of the Power System Under Test (PSUD). Finally, a time-domain and frequency domain accuracy analysis is conducted on experimental results to demonstrate the potential of the proposed infrastructure.**

***Index Terms*—Power System Analysis, Smart Grid, Digital Real-time Simulators, Co-simulation Techniques, Numerical Stability.**

I. Introduction

In the last few years, a robust research effort has been given to computer-aided power system analysis for designing, developing and testing future Smart Grid. Different domain-specific software simulation tools have been developed to emulate innovative functionalities and/or specific components of innovative power networks with high precision and accuracy [1]. For instance, time-domain modelling such as Transient Stability (TS) and Electromagnetic Transient (EMT) analyses are crucial in the planning, design, and operation of modern power transmission systems.

Though the power of pure software simulation, the rising interest in testing real-world hardware focused power system researchers' attention on real-time simulation. Such a paradigm refers to a software model of a physical system that can execute at the same rate as the real-world physical system following the *wall clock* time. Simulations of such a paradigm are performed in a discrete constant time-stepped environment (i.e. fixed timestamp simulation) in which they must solve the internal state equation of the system under test in less time than the fixed timestamp duration. Conversely, an over-run error occurs.

The time constraint of a real-time simulation varies depending on the application required. Taking a power flow analysis as an example, it does not require strict timing due to its simple calculation required. Vice versa, EMT requires around tens of microseconds fixed timestamp duration to depict the detailed dynamics of large AC systems [2]. To this purpose, innovative multiprocessor architecture (e.g. IBM® Power8) and Field Programmable Gate Array (FPGA) have been proposed as a suitable solution to ensure hardware acceleration of EMT analysis [3] through dedicated parallelisation of the task required to fulfil Dommel algorithm for network solution [4] and to respect real-time constraints.

Moreover, such technologies ensure fast digital and analogue Input/Output (I/O) facilities to create the closed-loop interface with a real power system component allowing Power Hardware-In-the-Loop (PHIL) to test its functionalities in a protected environment (i.e. laboratory set-up). PHIL avoids huge costs in deploying such a component in the real-world and shortens its design cycle. Nevertheless, PHIL is subject of stability and accuracy issues due to the latency of communication and power amplifier harmonic distortions between the power Device Under Test (DUT) and the simulated Rest Of the System (ROS) that could lead to serious damage of the hardware involved. Fortunately, different Interface Algorithms (IA) have been proposed in the literature to mitigate the effect of communication latency and stabilise the overall system under test [5].

Different commercial real-time simulators have been proposed to support power system designer in addressing

such complex analyses and to allow secure PHIL, so-called Digital Real-Time Simulators (DRTS). The main difficulty for such DRTS is the significant computational resources required for the solution of detailed EMT models thereby limiting the size of AC system that can be accurately simulated [6]. In fact, a growing effort of power system research community is concentrating on combining two or more DRTS exploiting novel methodologies, communication protocols and standard [7], such as co-simulation techniques. Such techniques allow splitting the power system network under analysis into sub-networks each one executed on a DRTS exploiting high-bandwidth communication channel (e.g. IEEE 802.3) to exchange interface voltages and currents between each other. However, such interconnections could lead to numerical instability and accuracy due to communication latency among DRTS like in the case of PHIL.

In this paper, the authors present a frequency-domain stability and time-domain accuracy analysis of the point-to-point interconnection of two commercial DRTS (i.e. RTDS Technologies Novacor2). This test-bed will foster future design of a distributed real-time co-simulation infrastructure allowing PHIL testing. This architecture will aim at extending the Power System Under Test (PSUD) scalability by splitting it on different DRTS exchanging data through communication protocols.

Firstly, the communication latency among the two DRTS is calculated on the proposed test-bed exploiting the fastest available on-board communication protocol (i.e. Aurora 8B/10B). Communication latency modifies the overall PSUD behaviour causing instability and inaccuracies of the electric network solution. So, a theoretical study inspired to PHIL IA is proposed to assess the frequency-domain stability constraints of a simple power system circuit split in the two DRTS. On the basis of this study, a PHIL IA will be applied to DRTS interconnection. Finally, calculated latency and theoretical results will be exploited to undertake experiments of such DRTS interconnection and to test the time-domain and frequency-domain accuracy of the co-simulation solution.

The structure of this paper is as follows. Section II provides a review on DRTS architecture. Then, it will follow a literature review on frequency-domain stability and time-domain accuracy analysis of PHIL IA that inspired our theoretical analysis on DRTS interconnection. Section III provides a comprehensive description of the co-simulation challenges still open. This Section also describes the test-bed and the two conducted experiments, namely *i)* the latency calculation of the Aurora communication protocol, and *ii)* the application of PHIL Ideal Transformer Method (ITM) IA to the proposed test-bed to undertake a frequency-domain stability analysis of a general DRTS interconnection. Section IV presents the results of the experiments to demonstrate the time-domain and frequency-domain accuracy of the proposed solution. Finally, Section V reports concluding remarks and future works.

II. Related Works

Time-domain analysis (e.g. EMT) of large AC transmission network require significant computational power to reduce the simulation timestamp, enlarge network sizes, and accurately capture its high frequency transients. For EMT analysis, a widely accepted and well used pure software solution is Electromagnetic Transients Program (EMTP) [4] that implements Dommel algorithm for the network solution. But the requirements for real-time simulation make it necessary to exploit parallel computing architecture. Different works analysed multi-DSP [8]–[10], multi-RISC [11], PC-cluster architectures [12], [13] and FPGA solution. For instance, Chen et al. [14] present a FPGA-based real-time EMTP simulator based on a deeply pipelined paralleled Dommel algorithm.

In the last decade, different commercial real-time power network simulators have gained the interest of power system designer to address real-time constraint and apply PHIL testing. The most important DRTS producers for power system analysis are: *i)* RTDS Technology, and *ii)* Opal-RT. In particular, RTDS Technology proposes Novacor2 chassis, a POWER8 RISC 10-core architecture capable of continuous real-time EMT. Different plug-and-play external boards enable Digital I/O, Analogue I/O and standard communication protocols for power system (e.g. PMU, GOOSE, IEC61850) widening its scope of application. Finally, RTDS provides RSCAD, a cohmprensive software GUI to design complex power system scenario.

However, RTDS suffers a limited number of node that restrict the scalability of the Power System Under Test (PSUD). Different works have proposed to relax the complexity of the simulation of some part of the power network in analysis and scale up the PSUD, so called Multi-rate approach [15]. Multi-rate approach proposes to define different time resolution separating the PSUD analysis in...**explanation of multi-rate, HV and MV? Long line???** ... but still the scalability is limited.

To cope with such a limitation, power system research community start proposing to interconnect together different DRTS exploiting fast high-bandwidth communication protocols (e.g. TCP and UDP protocol stacks). But even with these optimistic premises, DRTS interconnection suffers a series of inaccuracies due to time latencies, jitter, limited bandwidth, and network interface management of the communication link among different DRTS. These inaccuracies could affect stability of a PSUD co-simulation like happen in PHIL system when trying to interconnect a DUT to a simulated ROS. In fact, PHIL introduces several criticalities with error (i.e. time delay and power amplifier harmonics distortion) generated by the power interface that may cause severe instability issues or unacceptably inaccurate results. These effects are comparable to DRTS interconnection ones.

In [16], Ren et al. present the PHIL instability problem highlighting the importance of closed-loop stability improved from a particular Interface Algorithm (IA). In [5], the most interesting IAs are compared together: *i) Ideal Transformer Model* (ITM) and its variants [17]–[19], and *ii) Damping Impedance Method* (DIM) with different estimation algorithm of the damping impedance size [20], [21]. The outcome of this comparison highlights that ITM is the straightforward and the simplest IA to overcome instability and inaccuracies of the PHIL application.

So, the common thread of the proposed analysis is inspired from theory of PHIL application. The novelty of this paper is applying ITM IA to DRTS co-simulation infrastructure. Exploiting ITM IA, we could obtain better accuracy and stability of the PSUD numerical solution. This is demonstrated by following the Nyquist principles of frequency-domain analysis commonly used in PHIL context to determine the stability of IAs. Furthermore, the application of the fastest communication protocol ensure the lowest communication latency, ensuring the lowest non linear effect on the PSUD numerical solution originated by the ITM IA application. The proposed frequency-domain and time-domain analysis fund the basis for the application of co-simulation infrastructure in power system analysis.

III. Methodology

Co-simulation is a flexible approach to integrate different domain specific simulators together in a shared and distributed simulation environment. Following this paradigm, a complex scenario is decomposed in a system of systems topology in which each node (i.e. subsystem) is simulated by a different simulator engine (or solver). This decomposition allows to choose among a set of domain specific simulation tools to find the best solution that enhance numerical calculation and boost computational time of a single subsystem. For instance, Digital Real-Time Simulators (DRTS) is a plus to fulfil a Smart Grid simulation in a distributed co-simulation infrastructure.

Co-simulation approach must preserves high efficiency and accuracy in each single subsystem simulation. Furthermore, the complex dynamic system of systems simulation obtained by coupling different simulator may not cause instability and inaccuracies that could be caused by its application. The main challenges in this regards are: *i) Time Synchronisation and Regulation*, and *ii) Communication.*

Time Synchronisation is mandatory when the distributed co-simulation infrastructure interact in a time-dependent manner. It refers to the algorithm used to ensure temporally correct ordering among events generated by various simulators. *Time Regulation* instead refers to the need of instituting a policy to regulate how individual simulators evolve time. For instance, a particular simulator could be leader of the distributed environment (i.e. time-regulating), some others could be follower (i.e. time-constrained). Depending on the application, a policies must be created using a correct time regulation scheme for the simulators involved, which can have a major impact on performance and correctness of the distributed co-simulation environment.

Time Synchronisation and Regulation issue could be neglected choosing the right time regulation schema and synchronising the starting point of each subsystem simulation. In real-time world, each DRTS normally manages independently time evolution to fulfil its real-time constraint and cannot be controlled from external source. So, the best time regulation schema is setting all node as time-regulating ones. The evolution in time is ensured by considering each DRTS independent by each other and following the same wall clock time. Synchronisation instead is important to run specific PSUD that requires...**which ones?**. This task is ensured by the application of network time protocols (e.g. IEEE 1588 Precision Time Protocols) that align internal DRTS clocks and run each subsystem with a common wall clock starting time.

On the other hand, *Communication* refers to data exchange among different interconnected simulators, normally carried out by telecommunication protocols. Choosing the right protocol is fundamental to design an accurate and reliable co-simulation infrastructure capable of ensuring stability of the numerical solution. The main issues are normally generated by latency (or lag). In co-simulation context, latency is the time delay between the sending procedure of data retrieved from a simulator engine and the receiving procedure that present the received data into the solver of other distributed simulator environments to fulfil their numerical calculation. Latency is the main cause of instability and inaccuracies for a distributed co-simulation infrastructure and must be mitigated applying specific techniques.

In the following subsections, two experiments are described: *i)* the communication latency calculation of the proposed co-simulation infrastructure, and *ii)* the application of the Ideal Transformer Model IA on a simple electric test case to address its frequency stability and time accuracy analysis.

A. Communication Latency

Communication strongly affects numerical stability of DRTS co-simulation infrastructures introducing latency due to the telecommunication protocols that are normally used to apply co-simulation techniques (e.g. TCP and UDP protocol stacks).

The co-simulation infrastructure proposed in Figure 1 reduces significantly the latency between two DRTS simulation environment exploiting Aurora 8B/10B protocol. Aurora is a high performance lightweight link-layer protocol developed by Xilinx to exchange data across a point-to-point serial link with a low communication latency. On the RTDS Novacor2 rack employed for the tests, Aurora implementation chooses a single 2-width lane with a framing interface capable of reaching a line rate of

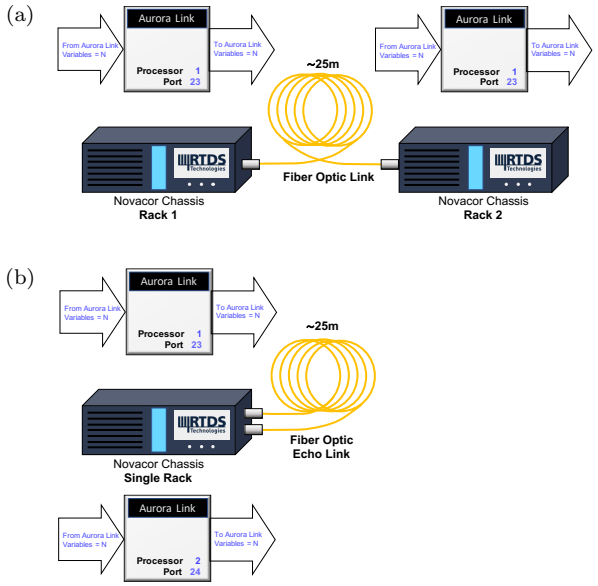


Fig. 1. Distributed DRTS co-simulation infrastructure (a) exploiting an Aurora 8B/10B link through an optical fiber cable of 25 meters length and its virtual implementation (b) setting an echo link between two different SFP port of a single Novacor2 rack.

2Gbps with a duplex communication w/o flow control. The frame is completely configured by the end user choosing a variable sequence of integer and 32-bit float. Apart from data formats, it has no particular restrictions.

In Figure 1a, two RTDS Novacor2 racks have been coupled with a 25 meters optical fiber link exploiting Aurora protocol. Aurora could be enabled in RSCAD by using the *_rtds_aurora* block, so called *Aurora block*. This block permits to define the Selected small form Factor Pluggable (SFP) transceiver port, the processor number, a priority level of computation, the frame definition (i.e. exchanged environment variables) and the sequence number blocking property of the Aurora link. More in depth on sequence number blocking activation, it minimise the loop delay between the communicating RTDS Novacor2 racks. In fact, the sequence number is a counter that is always appended to each frame. Once sequence number blocking property is activated, each rack must take the sequence number it receives and echo it back at the end of the response frame that is sent back to the sender and vice versa. The response of the echoed answer with the received sequence number must be fairly quick and less than the fixed simulation timestamp. Since a one-way communication latency take only 1100 ns in RTDS Novacor2 rack, this restriction is always respected.

However, latency in the numerical solution varies in respect to this value due to the complex Power8 RISC 10-core architecture implemented in RTDS Novacor2 rack. In fact, the most significant latency components are caused by the variables exchanged between control signals core and network solution cores. Control signal core is in charge of managing control variables, like data received from Aurora. Network solution cores instead solves the differential equation of the proposed PSUD applying network variables (i.e. voltages and currents) to the impedance matrix of the system. Different timestamp of simulation could be required to pass through control variables from control core to network variables in the network solution core. So this co-simulation infrastructure set-up allows a precise calculation of the latency generated by the overall communication process, not only the telecommunication protocol one.

As depicted in Figure 1b, a single rack has been used to avoid complex time regulation and synchronisation schema. The DRTS interconnection could be virtually deployed on a single rack exploiting Aurora protocol between two different SFP transceiver ports (i.e. 23, 24). To avoid conflict with the sequence number blocking setting, each Aurora block must be assigned to a different processor (i.e. 1, 2).

B. Ideal Transformer Model IA

Communication latency is normally experienced in PHIL application with similar effects to co-simulation application. In PHIL context, a monolithic electric system (see Figure 2a) is split exploiting a voltage divider into *i)* a real hardware Device Under Test (DUT), and *ii)* a simulated Rest Of the System (ROS). However, the voltage divider is not ideal since the power interface (i.e. power amplifier) and the sensors to retrieve real measurements between the ROS and the DUT may experience delays and errors (e.g. offset, harmonics distortion, nonlinearities, etc.). Specific techniques must be applied to ensure stability and accuracy of the overall PHIL system, so called *Interface Algorithm* (IA).

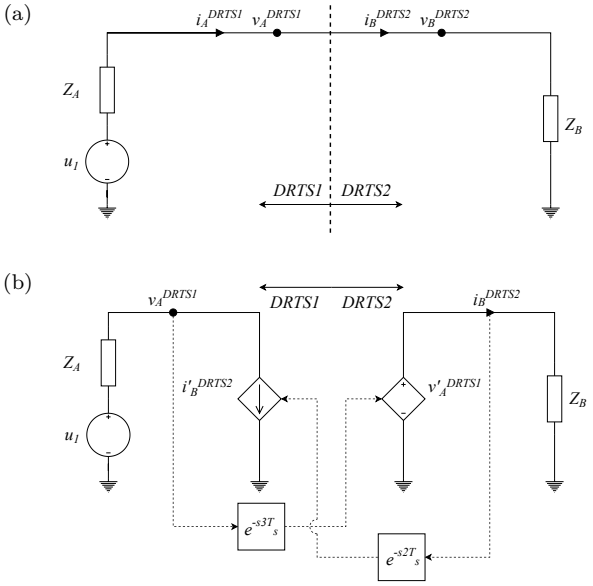


Fig. 2. Monolithic electric circuit (a) composed by an AC voltage source u_1 and two impedances Z_A and Z_B and the application of ITM IA (b)

In particular, the Ideal Transformer Method (ITM) described in Figure 2b is the simplest and effective IA to ensure stability of a PHIL system. ITM exploits a controlled voltage generator in the right part of the circuit that reproduce the voltage v_A to the left part (i.e. v'_A), and a current generator in the left part of the circuit to exchange the current i_B to the right part (i.e. i'_B). Moreover, it applies a latency that is proportional to the latency experienced by the exchanged variable from ROS to DUT to take effect on the DUT circuit (i.e. T_{D_1}) and vice versa (i.e. T_{D_2}).

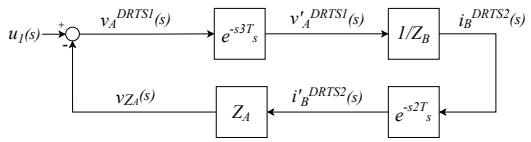


Fig. 3. Equivalent Block Diagram of the ITM IA

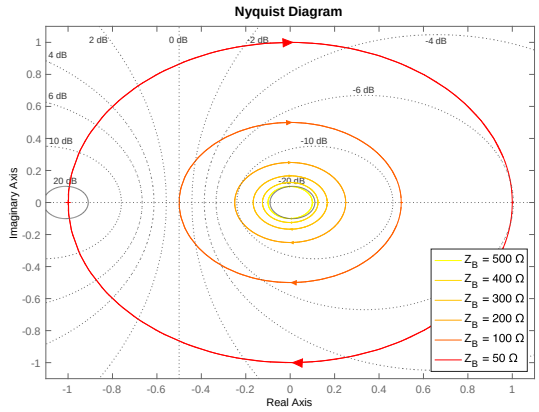


Fig. 4. Nyquist diagrams of the open-loop transfer function G_{ol} for $Z_B = 50, 100, 200, 300, 400$, and 500 Ω

In Figure 3, the equivalent block diagram of the ITM circuit could lead us to its frequency-domain stability analysis. Exploiting ITM open-loop function described by Equation 1, the Nyquist diagram is calculated for $Z_A = 50\ \Omega$ and different values of Z_B, namely $50, 100, 200, 300, 400$, and 500 Ω. Following the Nyquist criterion, the Nyquist diagram of the open loop function of ITM system must not encircles the critical point $(-1, 0)$ to ensure its stability. As depicted in Figure 4, the ratio Z_A/Z_B must be minor than 1 to ensure the Nyquist criterion (Equation 2). Also in case stability is ensured by this criterion, a large latency could provokes nonlinearities (i.e. phase shift) that impact both frequency-domain and time-domain accuracy of the overall system.

$$G_{ol} = \frac{Z_A}{Z_B} e^{-s(T_d^1 + T_d^2)} \tag{1}$$

$$\frac{Z_A}{Z_B} < 1 \tag{2}$$

ITM IA could be applied also in DRTS interconnection and can help in study the effects of time-domain accuracy and frequency-domain stability of a co-simulation infrastructure. In fact, the novelty of this paper is applying ITM IA algorithm in DRTS interconnection to study stability and accuracy of the co-simulated PSUD. Applying the co-simulation infrastructure proposed in Figure 1b, the ITM IA has been applied in RSCAD model exploiting an Aurora link between RTDS Novacor2 SFP port 23 and 24.

IV. Analysis of Numerical Stability and Accuracy

In the following Section, two different experiments are described: *i)* Communication Latency Calculation, and *ii)* ITM IA application. Afterwards, the time-domain accuracy analysis and frequency-domain accuracy analysis is conducted over the result obtained by the ITM IA application.

A. Communication Latency Calculation

The results on the communication latency calculation have been carried out exchanging a reference clock through the Aurora link to calculate the difference with the receiving simulation time. The reference clock has been sent from 2 to 128 times for each simulation timestamp, that are the minimum and maximum values allowed to be exchanged following the specification of the RSCAD Aurora block. This set up has been repeated for different timestamp duration T_{Sim} from 10 µsec to 500 µsec.

T_{Sim} \ Var	2	...	128
10 µsec	0	0	0
...	0	0	0
500 µsec	0	0	0

TABLE I
Co-simulation infrastructure latency results

Latency results 0 for all T_{Sim} values and all Var number of variables exchanged as described in Table I since the reference clock is a control variable and does not requires to be exchanged with the network solution cores. These results confirm the set-up of the co-simulation infrastructure described in Section III-A.

B. ITM IA Application

The ITM circuit described in Figure 2b has been reproduced in RSCAD software. The sinusoidal voltage source u_1 has been configured with a voltage magnitude of $100KV$ and an AC power supply frequencies of $50Hz$. Moreover, the pure resistive impedance Z_A has been fixed to 50 Ω. A metering point v_A is set to retrieve its voltage and will allow to export the network variable to the control core. This operation will take $1T_{Sim}$. Each timestamp, the exported control variables v_A is sent through the Aurora link on port 23 and received by the control core on the port

24. As previously demonstrate by the test in Section IV-A, this operation take no timestamp. The control variable received v'_A is imported into the network solution core and forces the controlled voltage source to generate v_a. This operation will take $2T_{Sim}$. The total latency for sending v_A to the right part of the circuit is $3T_{Sim}$.

In the right circuit, Z_B is set to two values, respectively *i)* 50.5 Ω to test ITM near the instability region, and *ii)* 500 Ω to present a stable ITM IA application. The current i_B flowing into the impedance Z_B is then exported to the control core, sent through Aurora from port 24 to port 23, and then applied to the controlled current source to generate i'_B. Since the controlled current source requires only $1T_{Sim}$ to fulfil the operation of exchanging the received Aurora variable from the control core to the network variable i'_B , this operation takes in total $2T_{Sim}$. So, the complete round-trip latency results $5T_{Sim}$.

The timestamp duration T_{Sim} has been changed from 50 µsec to 500 µsec to run different tests and analyse voltages v_A, v_B and currents i_A, i_B network variables for the two Z_B values. The monolithic electric circuit in Figure 2a has been run simultaneously to the ITM case to retrieve the correct voltages and currents, namely $v_A\hat{}real$ and $i_A\hat{}real$. Results of the test demonstrate that applying a T_{Sim} lower than 50 µsec ensure good time-accuracy results. The results presented in the next sections are obtained for the worst case scenario that is when T_{Sim} is set to 500 µsec. Only voltages results has been shown to avoid repetition since the $cos\phi = 1$ of a pure resistive circuit is 1 and currents and voltages are in phase.

C. Time-domain Accuracy Analysis

The ITM IA voltage result is compared with the monolithic electric circuit solution for both Z_B values to assess a quantitative time-domain accuracy of the numerical solution. The case $Z_B = 500\ \Omega$ is presented in Figure 5a. v_A (*green*) is overlying v_A^{real} (*blue*) confirming that the calculation in both cases are comparable with a 2.28% rise of the v_A voltage peak due to the latency experienced by i_B to be reflected on the left part of the ITM circuit. v_B (*orange*) instead present correctly a latency o 1500 µsec that is equal to $3T_{Sim}$. Also v_B experience a rise in respect to v_A^{real} following v_A trend.

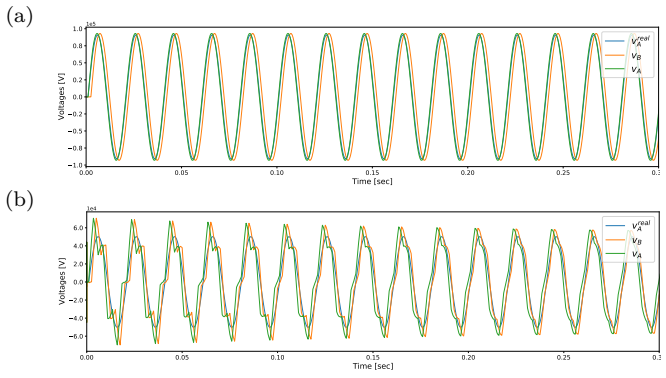


Fig. 5. Voltages time plots to compare time-domain accuracy of the monolithic circuit (*blue*) and ITM IA application (blue) for T_s = 500 µsec (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

The case $Z_B = 50.5\ \Omega$ in Figure 5b instead presents major voltages distortion. In fact, v_A present a distortion transient that is a direct effect of the phase shift due to the round trip latency of the ITM application equal to $5T_{Sim}$ and the magnitude of Z_A/Z_B equal to $0.\overline{9900}$. The initial peak of the distortion exceed the 40% in respect to v_A^{real}. v_B clearly follow the same v_A trend with a latency o 1500 µsec that is equal to $3T_{Sim}$. Moreover, the distortion transient presented in Figure 6a gets absorbed in 0.4 sec stabilising the result with an 7.92% rise in respect to the voltage arise of the case $Z_B = 500\ \Omega$. Furthermore, a distortion can be appreciated in Figure 6b due the effect of the phase shift generated by the identified latency that transform the pure sine in a non-linear one.

D. Frequency-domain Accuracy Analysis

The frequency-domain accuracy analysis is obtained applying the Welch's method for the Power Spectral Density (PSD) estimation to obtain a frequency description of the voltages signal results in both Z_B values. For $Z_B = 500\ \Omega$, v_A PSD overlying v_A^{real} peak at $f = 50\ Hz$ that is the power supply frequencies. Thus, the frequential content representation of the sine is correctly replicated as depicted in Figure 7a. The case $Z_B = 50.5\ \Omega$ instead present three different frequency peaks at $f = 200, 600,$ and 1000 Hz as well as the former peak at $f = 50\ Hz$.

The phase shift time-domain effect is similar to a triangle wave trend. A triangle wave can be approximated in time-domain with additive synthesis by Equation 3, summing odd harmonics of the fundamental sine wave of frequency f_Δ while multiplying every other odd harmonic by -1 and multiplying the amplitude of the harmonics by one over the square of their mode number n.

$$x_{triangle}(t) = \frac{8}{\pi^2} \sum_{i=0}^{N-1} (-1)^i n^{-2} sin(2\pi f_\Delta n t) \qquad (3)$$

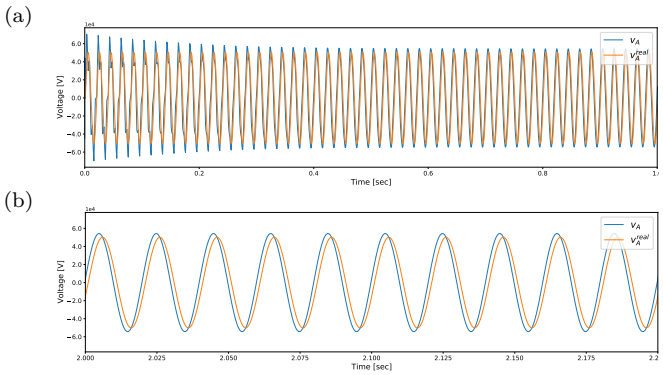
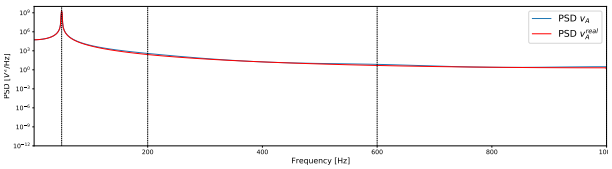


Fig. 6. Voltages time plots of (a) the transient when applying ITM IA for $T_s = 500$ µsec near the instability region $Z_B = 50.5\ \Omega$ and (b) its non linear effect on the numerical solution

(a)



(b)

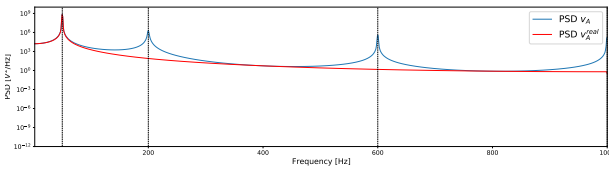


Fig. 7. Voltages Power Spectral Density (PSD) estimation applying Welch's method to compare frequency-domain accuracy of the monolithic circuit (*red*) and ITM IA application for $T_s = 500$ µsec (a) in the stability region ($Z_B = 500\ \Omega$), and (b) near the instability region ($Z_B = 50.5\ \Omega$)

Since each $5T_{Sim}$ the phase shift time-domain effect change signs, we can consider the fundamental sine wave period of the generated triangle wave T_Δ twice the round trip latency, resulting $10T_{Sim}$. As depicted in Equation 4, the fundamental frequency f_Δ is equal to inverse of the period T_Δ. Since T_Δ is equal to $10T_{Sim}$, the fundamental frequency f_Δ is equal to 200 Hz, confirming the empirical results. Consequently, the frequency of the odd harmonics are 600 Hz, 1000 Hz, and so on. This effect can be noticed clearly also for $Z_B = 500\ \Omega$ but mitigated by the magnitude of Z_A/Z_B equal to 0.1.

$$f_\Delta = \frac{1}{T_\Delta} = 200\ Hz \tag{4}$$

V. Conclusion

This paper present a stability and accuracy analysis of the proposed co-simulation infrastructure to interconnect DRTS together. It fund the basis on the PHIL fields, inheriting the ITM Interface Algorithm commonly used to ensure stability and accuracy of the analysis of DUT in such complex behaviour. The application of ITM IA to DRTS interconnection exploiting Aurora protocol ensures stability and accuracy of the numerical solution of a PSUD with the constraints $T_{Sim} \leq 50$ µsec and $Z_A/Z_B << 1$. A worst case scenario with $T_{Sim} = 500$ µsec has been analysed to assess the time-domain accuracy of the solution in both stability and near the instability. The ITM IA application ensure in both case an acceptable accuracy in reproducing the monolithic electric circuit. Since normal EMT analysis commonly uses smaller T_{Sim} around 50 µsec, we can assume that we can exploit the ITM application in DRTS interconnection to ensure the numerical stability in both region of interest.

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